CEC Continuing Education Center

DesignNews

Introduction to Multicore RTOS-based Application Development

DAY 3 : Digging into the Dual-Core STM32H7 MCU's

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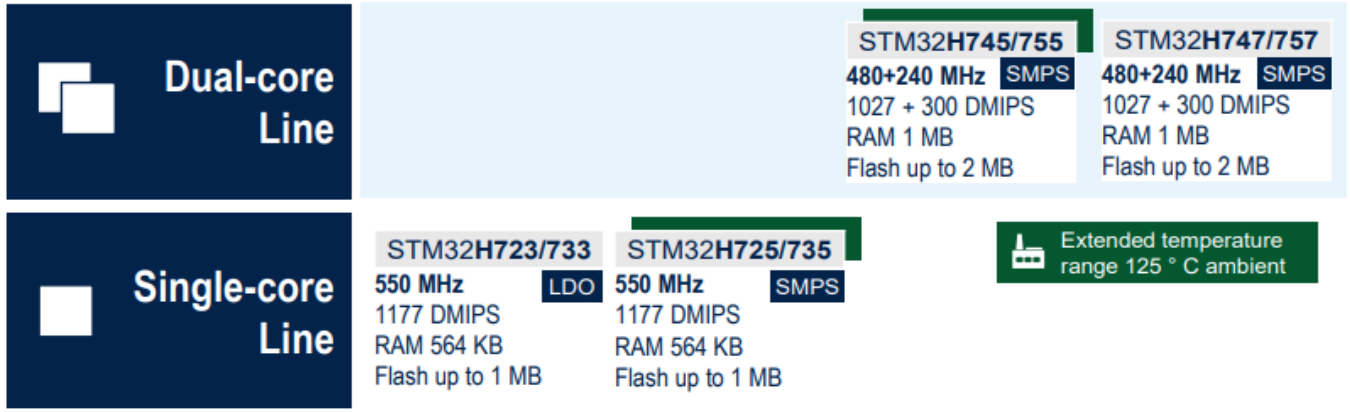
Course Sessions

- Multicore Application Architecture Design
- A Quick Review of RTOS Fundamentals
- Digging into the Dual-Core STM32H7 MCU's
- Toolchain Setup for Dual Core MCU's
- Writing Multicore Microcontroller Applications

STM32H7 Dual Core Microcontrollers

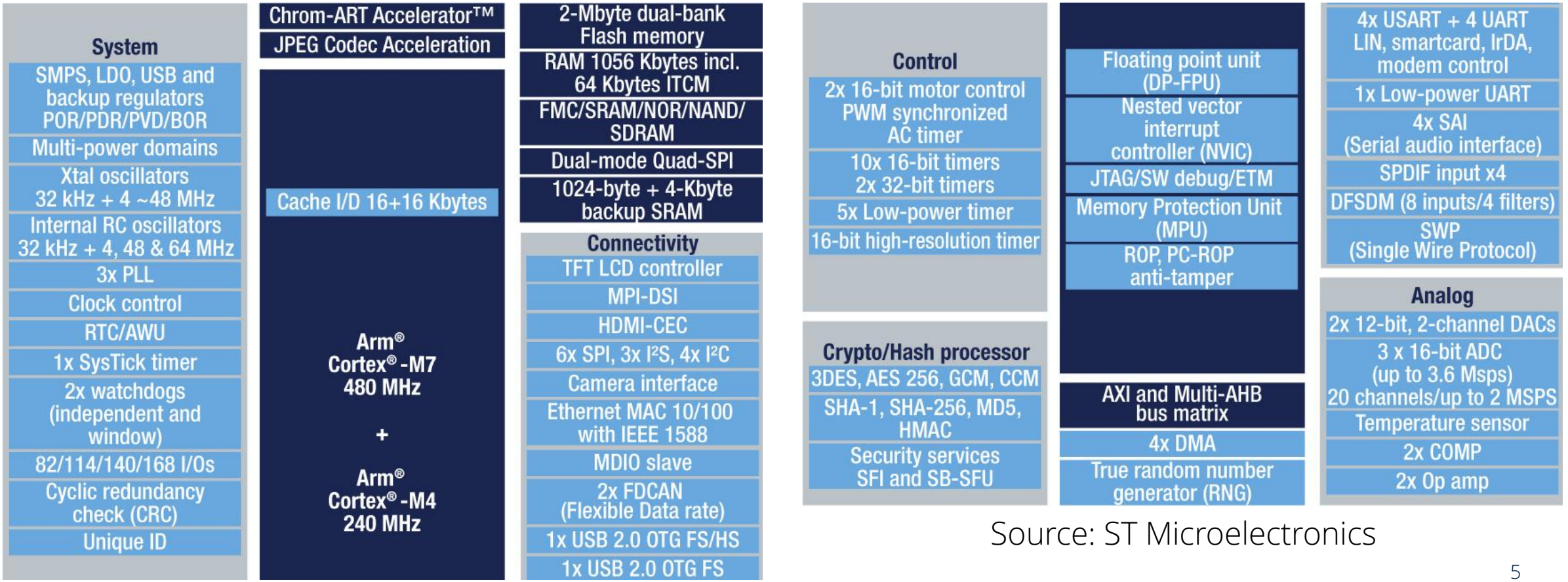
Overview

- Large Memory Footprint
  - 2 MB Flash
  - 1 MB of SRAM
- Cortex-M7 + Cortex-M4 core
  - 480 MHz
  - 240 MHz



Source: ST Microelectronics

STM32H7 Dual Core Microcontrollers



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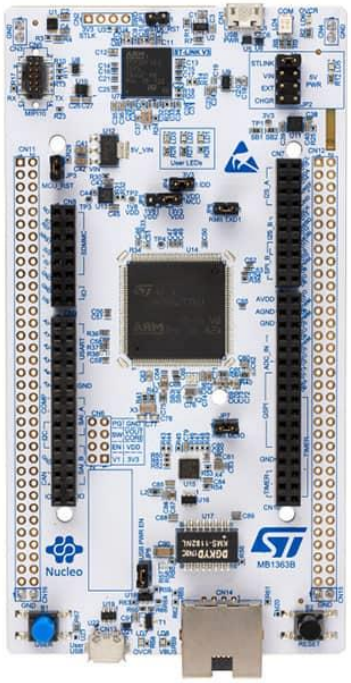
STM32 Dual Core MCU Development Boards

NUCLEO-H745ZIQ



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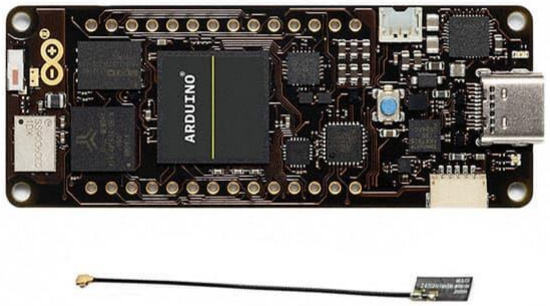
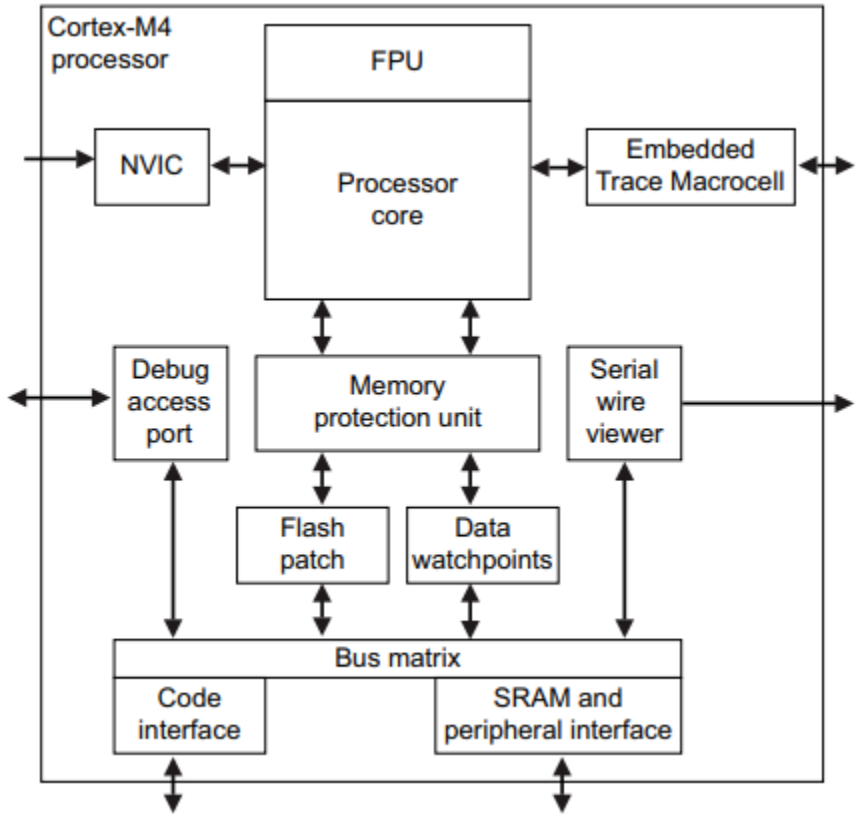


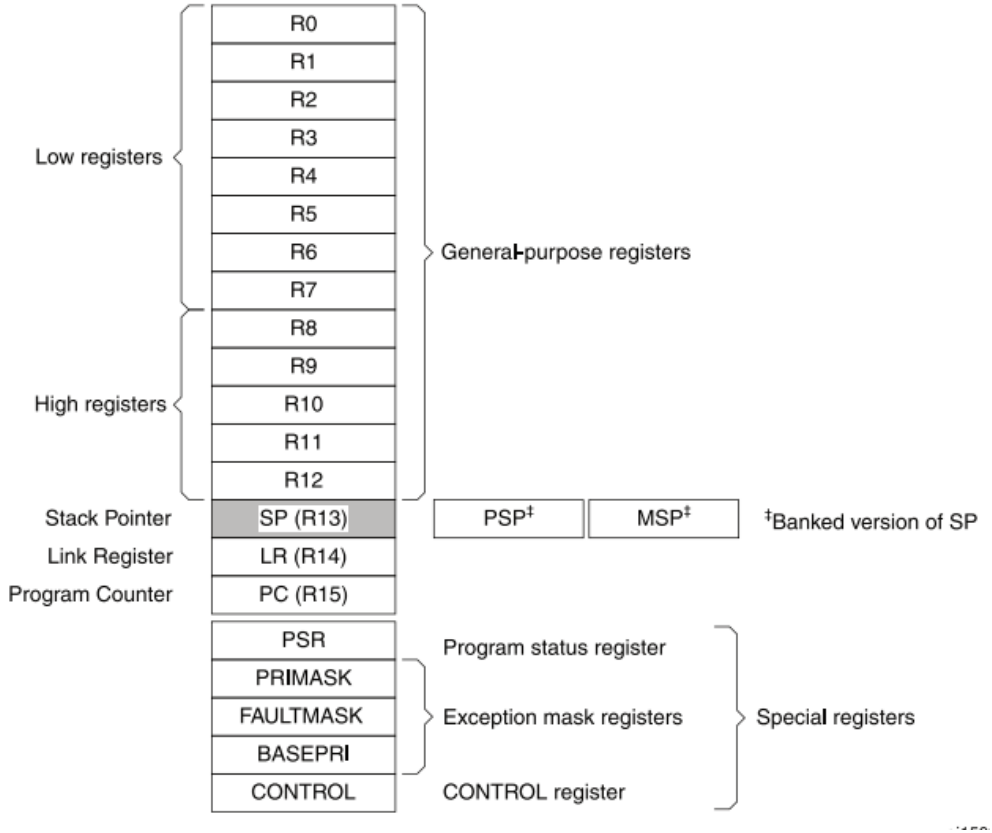
STM32H757I-EVAL

Will you be getting a development board to try out multicore microcontroller application development?

- Yes
- No

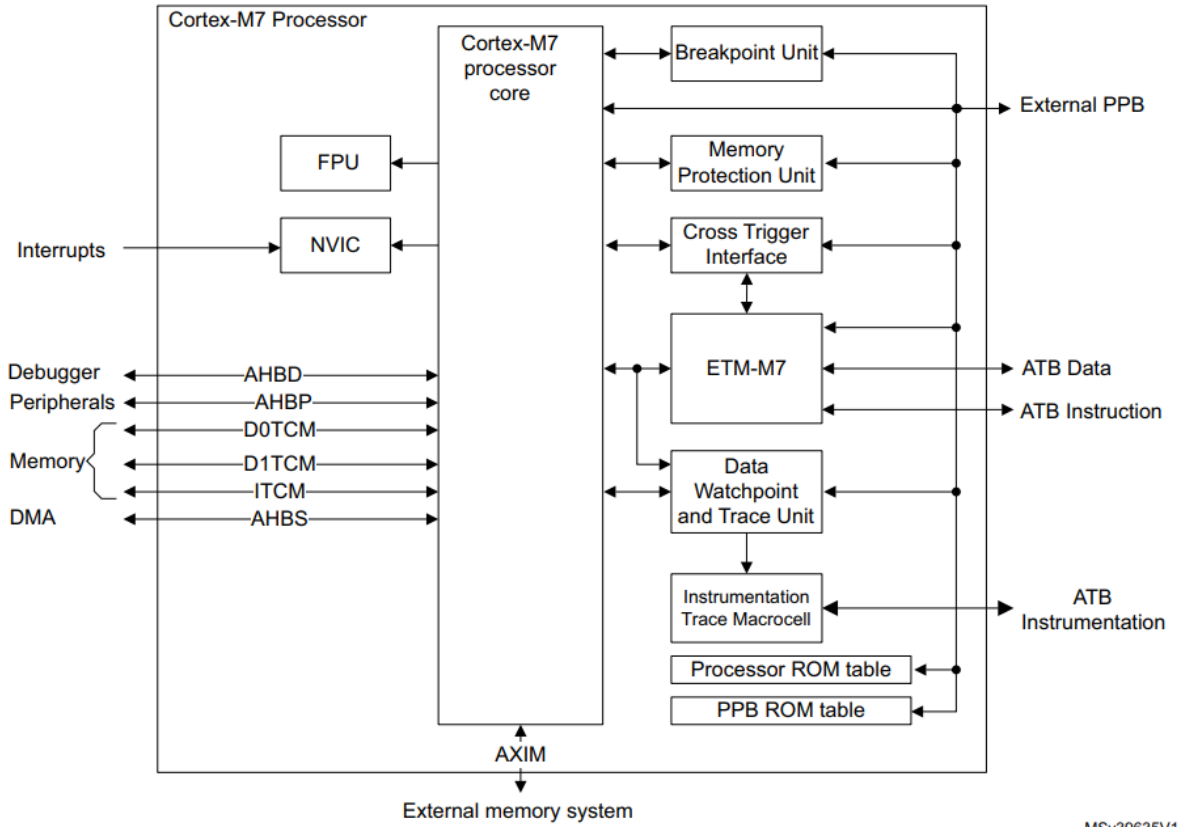
The STM32 Cortex-M4 Implementation

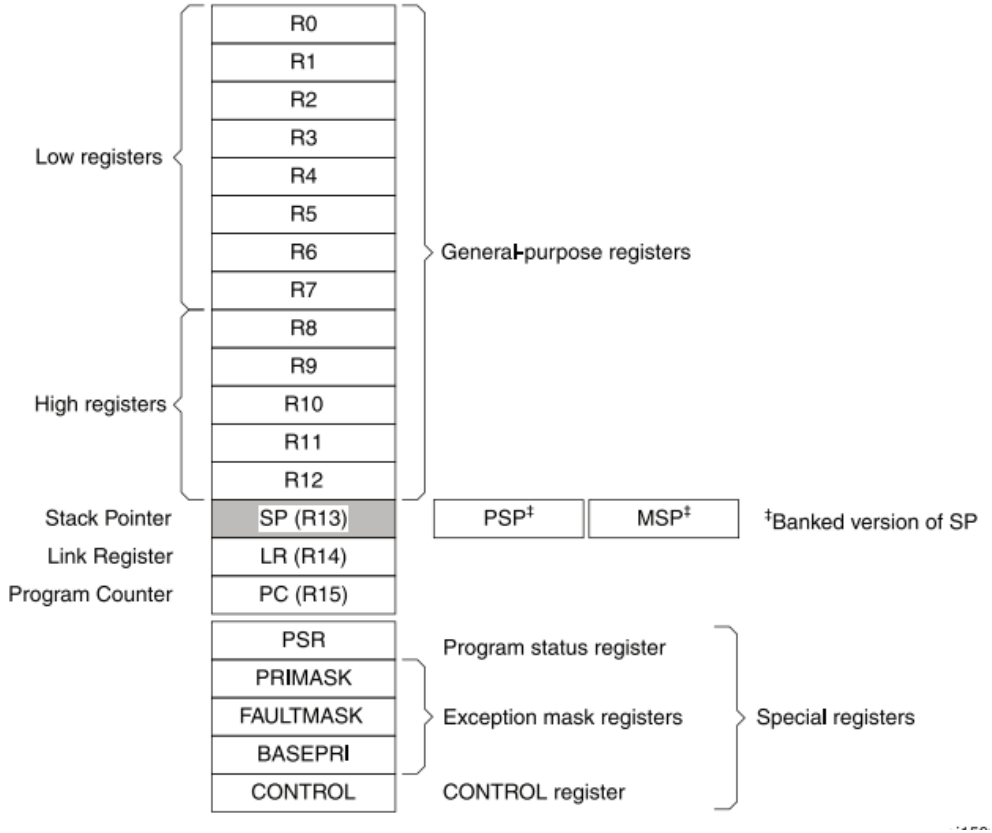




Cortex-M4 Programmers Manual: https://bit.ly/3s7KKmg

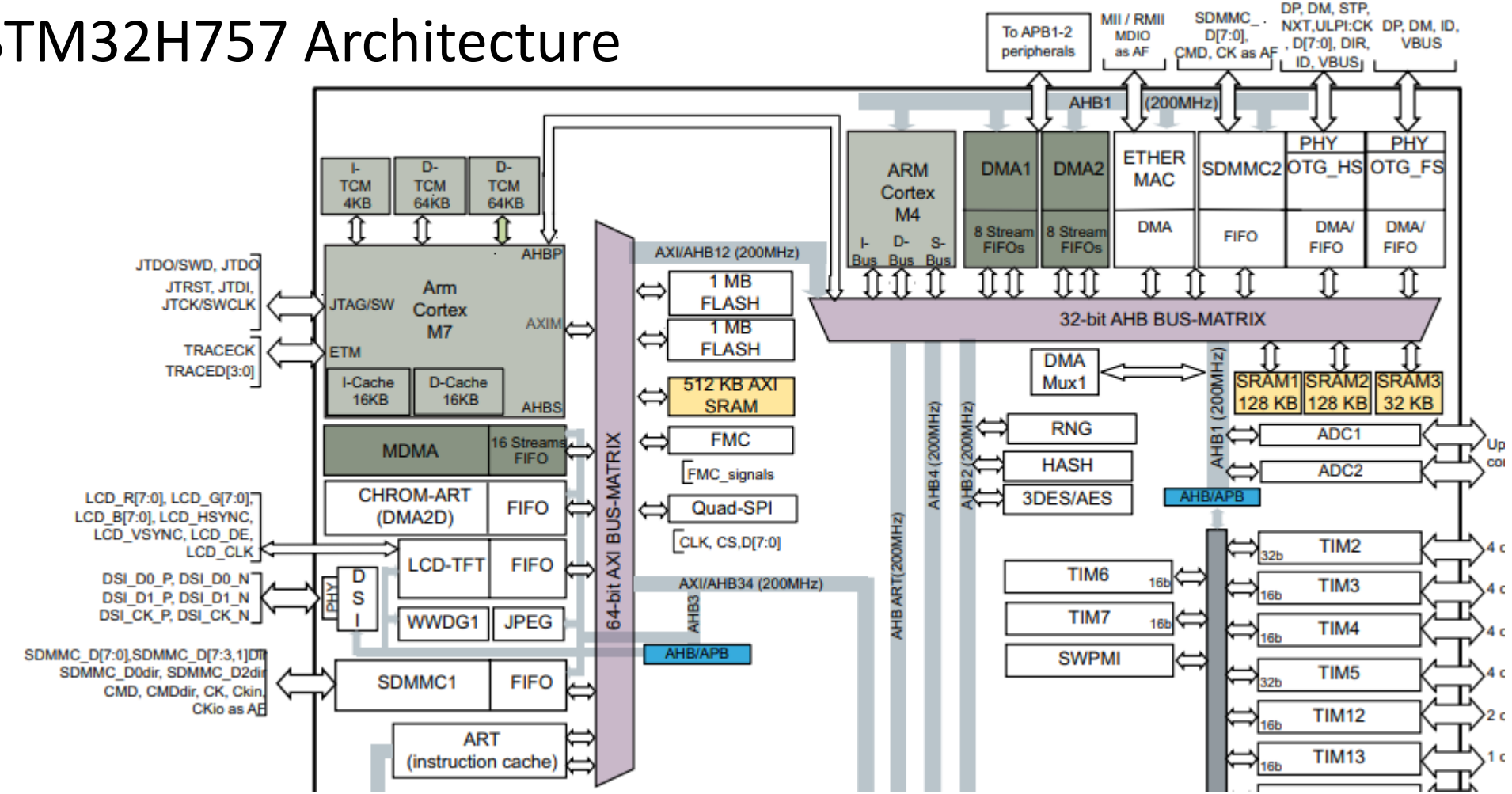
The STM32 Cortex-M7 Implementation





Cortex-M7 Programmers Manual: https://bit.ly/3pxAvpI

The STM32H757 Architecture



https://www.st.com/resource/en/datasheet/stm32h757zi.pdf Page 18

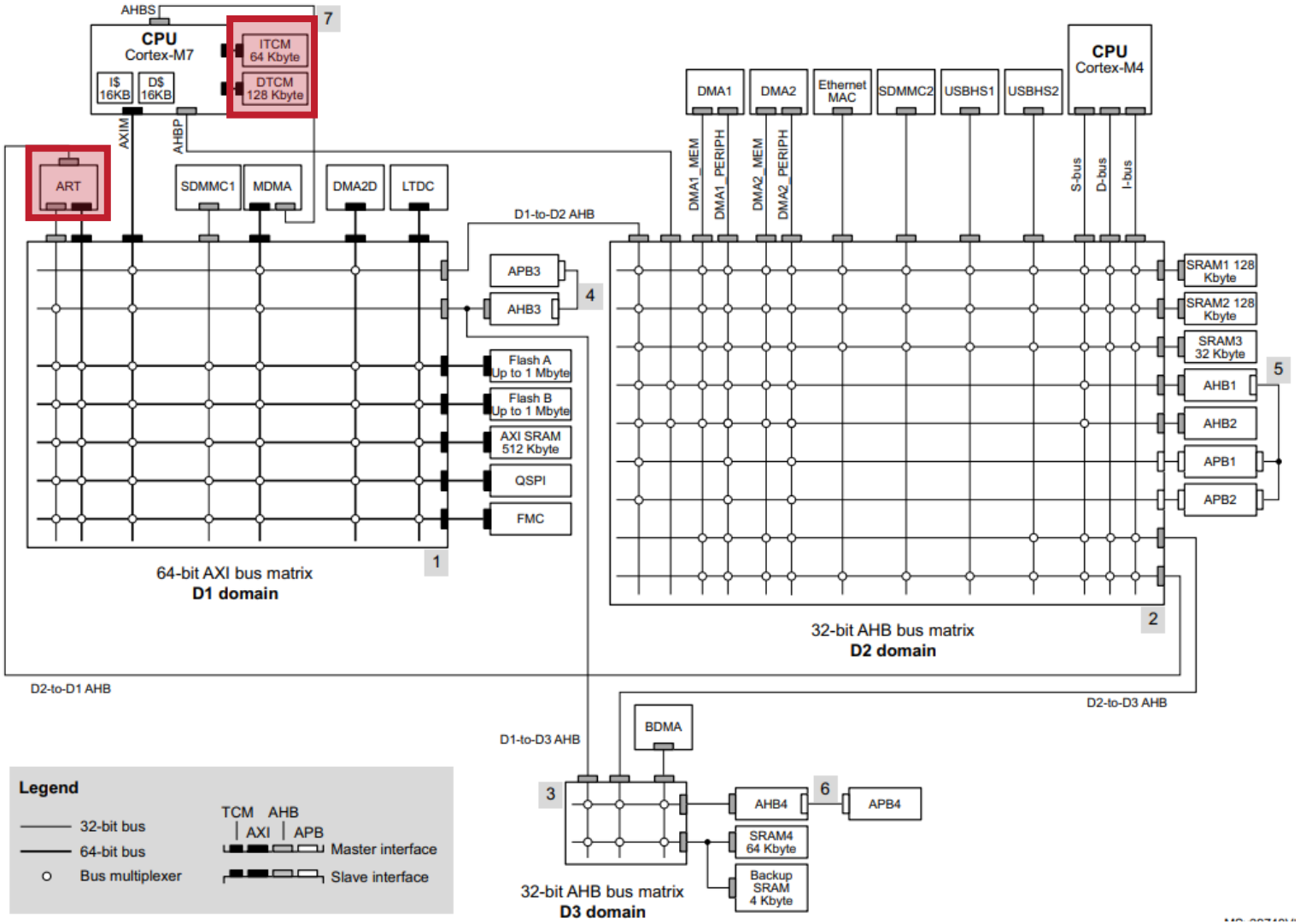


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Table 2. Bus-master-to-bus-slave interconnect

Bus slave / type[1]	Bus master / type[1]																				
	Cortex-M7 - AXIM	Cortex-M7 - AHBP	**Cortex-M7 - ITCM**	**Cortex-M7 - DTCM**	SDMMC1	**MDMA**	MDMA - AHBS	**DMA2D**	**LTDC**	DMA1 - MEM	DMA1 - PERIPH	DMA2 - MEM	DMA2 - PERIPH	Eth. MAC - AHB	SDMMC2 - AHB	USBHS1 - AHB	USBHS2 - AHB	Cortex-M4 - S-bus	Cortex-M4 - D-bus	Cortex-M4 - I-bus	BDMA - AHB
	Interconnect path and type[2]																				
ITCM	-	-	x	-	-	-	x	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DTCM	-	-	-	x	-		x	-	-	-	-	-	-	-	-	-	-	-	-	-	-
AHB3 periphs	x	-	-	-	-	x	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-
APB3 periphs	x	-	-	-	-	x	-	-	-	x	x	x	x	x	x	x	x	x	x	x	-
Flash bank 1	x	-	-	-	x	x	-	x	x	x	x	x	x	x	x	x	x	x	x	x	-
Flash bank 2	x	-	-	-	x	x	-	x	x	x	x	x	x	x	x	x	x	x	x	x	-
AXI SRAM	x	-	-	-	x	x	-	x	x	x	x	x	x	x	x	x	x	x	x	x	-
QUADSPI	x	-	-	-	x	x	-	x	x	x	x	x	x	x	x	x	x	x	x	x	-
FMC	x	-	-	-	x	x	-	x	x	x	x	x	x	x	x	x	x	x	x	x	-
SRAM 1	x	-	-	-	-	x	-	x	-	x	x	x	x	x	x	x	x	x	x	x	-
SRAM 2	x	-	-	-	-	x	-	x	-	x	x	x	x	x	x	x	x	x	x	x	-
SRAM 3	x	-	-	-	-	x	-	x	-	x	x	x	x	x	x	x	x	x	x	x	-
AHB1 periphs	-	x	-	-	-	x	-	x	-	x	x	x	x	-	-	-	-	x	-	-	-
APB1 periphs	-	x	-	-	-	x	-	x	-	x	x	x	x	-	-	-	-	x	-	-	-
AHB2 periphs	-	x	-	-	-	x	-	x	-	x	x	x	x	-	-	-	-	x	-	-	-
APB2 periphs	-	x	-	-	-	x	-	x	-	x	x	x	x	-	-	-	-	x	-	-	-
AHB4 periphs	x	-	-	-	-	x	-	-	-	x	x	x	x	x	x	x	x	x	-	-	x
APB4 periphs	x	-	-	-	-	x	-	-	-	x	x	x	x	x	x	x	x	x	-	-	x
SRAM4	x	-	-	-	-	x	-	-	-	x	x	x	x	x	x	x	x	x	-	-	x
Backup RAM	x	-	-	-	-	x	-	-	-	x	x	x	x	x	x	x	x	x	-	-	x

1. **Bold** font type denotes 64-bit bus, plain type denotes 32-bit bus.
2. "X" = access possible, "-" = access not possible, shading = access useful/usable.

A few useful definitions

ART accelerator – adaptive real-time memory access accelerator

ITCM-RAM – instruction trace ram can be accessed at maximum CPU clock without latency. Located on the Cortex-M7 at 0x0000 0000.

Which domain contains shared memory between the two cores?

- D1 Domain (High-Performance block)
- D2 Domain (Communication peripherals and timers)
- D3 Domain (reset/clock control/power management)

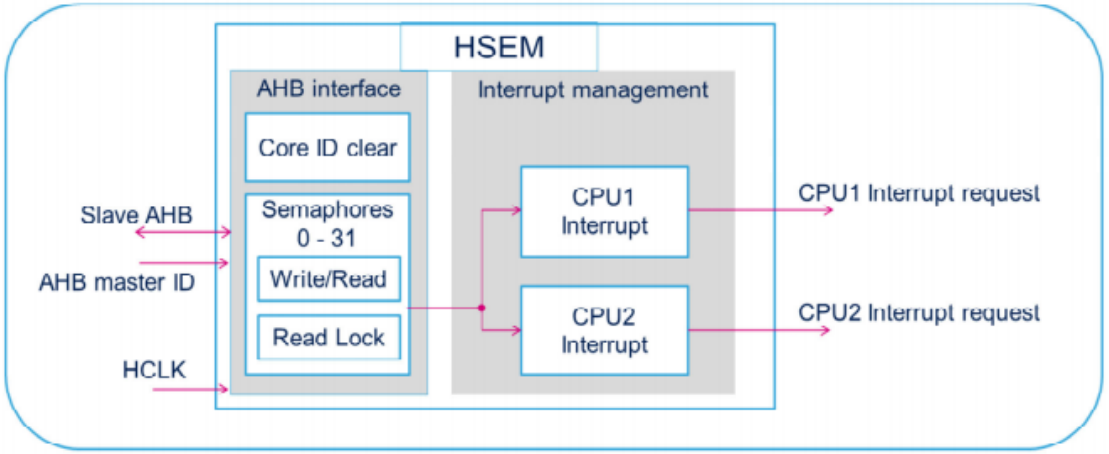
Processor Boot Options

- Simultaneous Boot (CM4 and CM7)
- Boot CM4 (CM7 Gated)
- Boot CM7 (CM4 Gated)

The HSEM Peripheral

HSEM is a hardware semaphore module used to manage access permissions and synchronization of resources between multiple processes.

- 32 Semaphores
- Multiple locking mechanisms
  - 1 step read lock
  - 2 step write, read back lock
- Located on the AHB interface bus



Source: STM

What are some possible applications for the HSEM?

- Used prior to a peripheral access
- Manage shared resources
- Synchronize processes
- All the above
- None of the above

Thank you for attending

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