



DesignNews

Introduction to Multicore RTOS-based Application Development

DAY 3 : Digging into the Dual-Core STM32H7 MCU's

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Course Sessions


- Multicore Application Architecture Design
- A Quick Review of RTOS Fundamentals
- **Digging into the Dual-Core STM32H7 MCU's**
- Toolchain Setup for Dual Core MCU's
- Writing Multicore Microcontroller Applications

STM32H7 Dual Core Microcontrollers

Overview

- Large Memory Footprint
 - 2 MB Flash
 - 1 MB of SRAM
- Cortex-M7 + Cortex-M4 core
 - 480 MHz
 - 240 MHz

 Dual-core Line	STM32H745/755 480+240 MHz SMPS 1027 + 300 DMIPS RAM 1 MB Flash up to 2 MB	STM32H747/757 480+240 MHz SMPS 1027 + 300 DMIPS RAM 1 MB Flash up to 2 MB
 Single-core Line	STM32H723/733 550 MHz LDO 1177 DMIPS RAM 564 KB Flash up to 1 MB	STM32H725/735 550 MHz SMPS 1177 DMIPS RAM 564 KB Flash up to 1 MB

 Extended temperature range 125 °C ambient

Source: ST Microelectronics

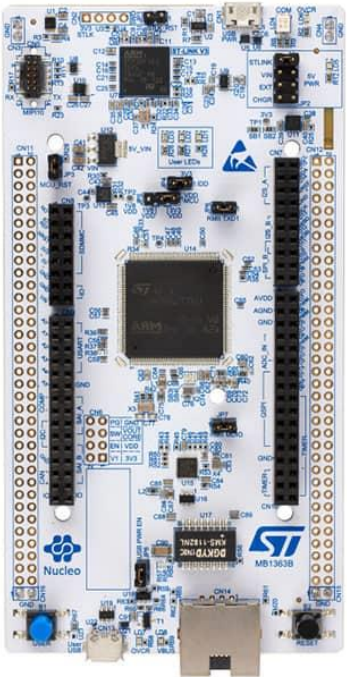
STM32H7 Dual Core Microcontrollers

<p>System</p> <ul style="list-style-type: none"> SMPS, LDO, USB and backup regulators POR/PDR/PVD/BOR Multi-power domains Xtal oscillators 32 kHz + 4 ~48 MHz Internal RC oscillators 32 kHz + 4, 48 & 64 MHz 3x PLL Clock control RTC/AWU 1x SysTick timer 2x watchdogs (independent and window) 82/114/140/168 I/Os Cyclic redundancy check (CRC) Unique ID 	<ul style="list-style-type: none"> Chrom-ART Accelerator™ JPEG Codec Acceleration Cache I/D 16+16 Kbytes Arm® Cortex® -M7 480 MHz + Arm® Cortex® -M4 240 MHz 	<ul style="list-style-type: none"> 2-Mbyte dual-bank Flash memory RAM 1056 Kbytes incl. 64 Kbytes ITCM FMC/SRAM/NOR/NAND/SDRAM Dual-mode Quad-SPI 1024-byte + 4-Kbyte backup SRAM Connectivity TFT LCD controller MPI-DSI HDMI-CEC 6x SPI, 3x I²S, 4x I²C Camera interface Ethernet MAC 10/100 with IEEE 1588 MDIO slave 2x FDCAN (Flexible Data rate) 1x USB 2.0 OTG FS/HS 1x USB 2.0 OTG FS 	<ul style="list-style-type: none"> Control 2x 16-bit motor control PWM synchronized AC timer 10x 16-bit timers 2x 32-bit timers 5x Low-power timer 16-bit high-resolution timer Crypto/Hash processor 3DES, AES 256, GCM, CCM SHA-1, SHA-256, MD5, HMAC Security services SFI and SB-SFU 	<ul style="list-style-type: none"> Floating point unit (DP-FPU) Nested vector interrupt controller (NVIC) JTAG/SW debug/ETM Memory Protection Unit (MPU) ROP, PC-ROP anti-tamper AXI and Multi-AHB bus matrix 4x DMA True random number generator (RNG) 	<ul style="list-style-type: none"> 4x USART + 4 UART LIN, smartcard, IrDA, modem control 1x Low-power UART 4x SAI (Serial audio interface) SPDIF input x4 DFSDM (8 inputs/4 filters) SWP (Single Wire Protocol) Analog 2x 12-bit, 2-channel DACs 3 x 16-bit ADC (up to 3.6 Msps) 20 channels/up to 2 MSPS Temperature sensor 2x COMP 2x Op amp
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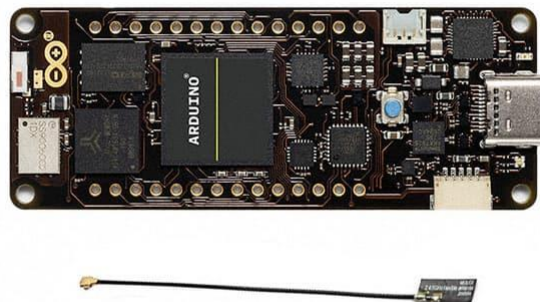
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STM32 Dual Core MCU Development Boards

NUCLEO-H745ZIQ



ABX00042



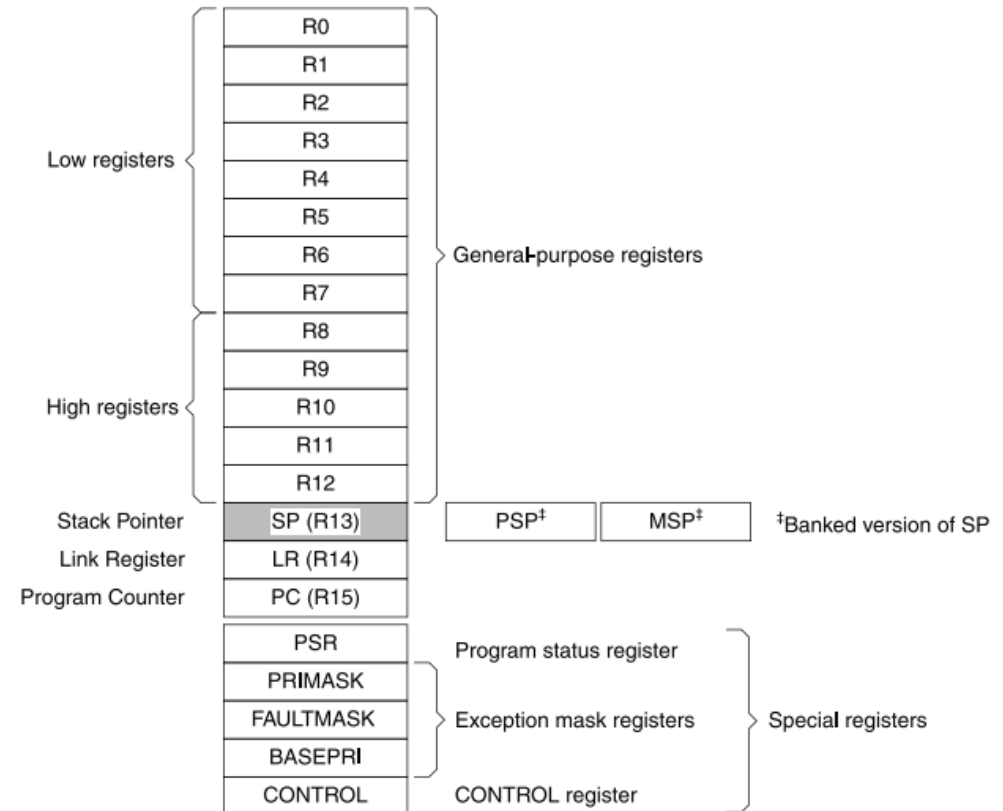
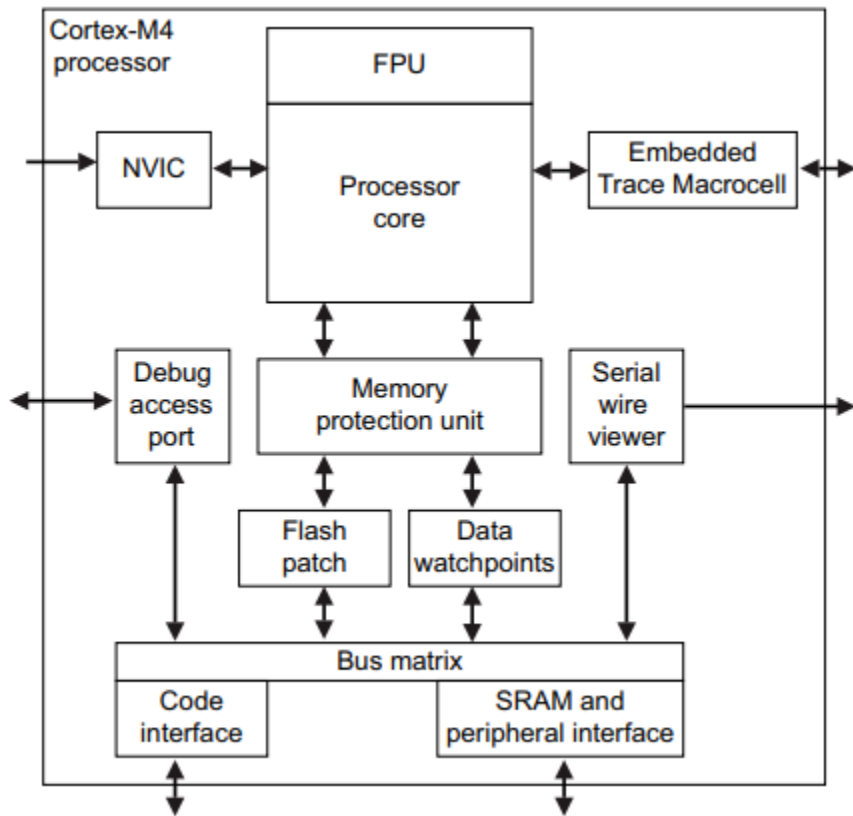
STM32H757I-EVAL



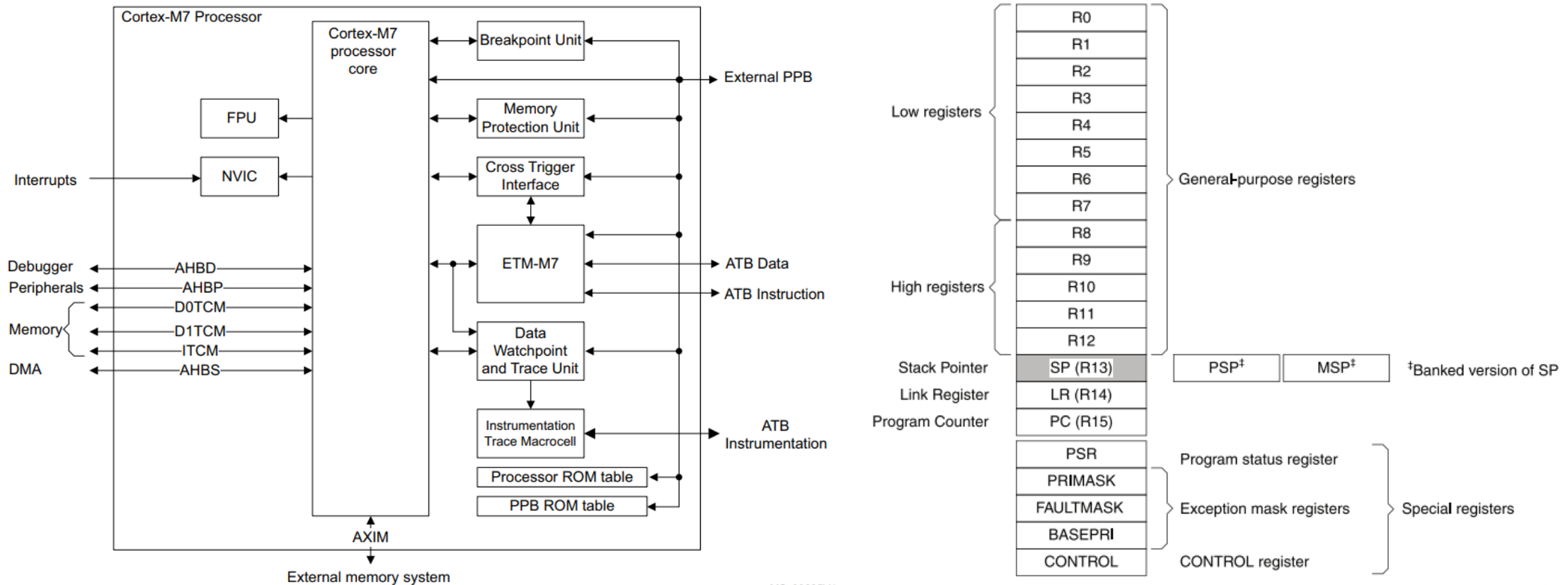
Will you be getting a development board to try out multicore microcontroller application development?

- Yes
- No

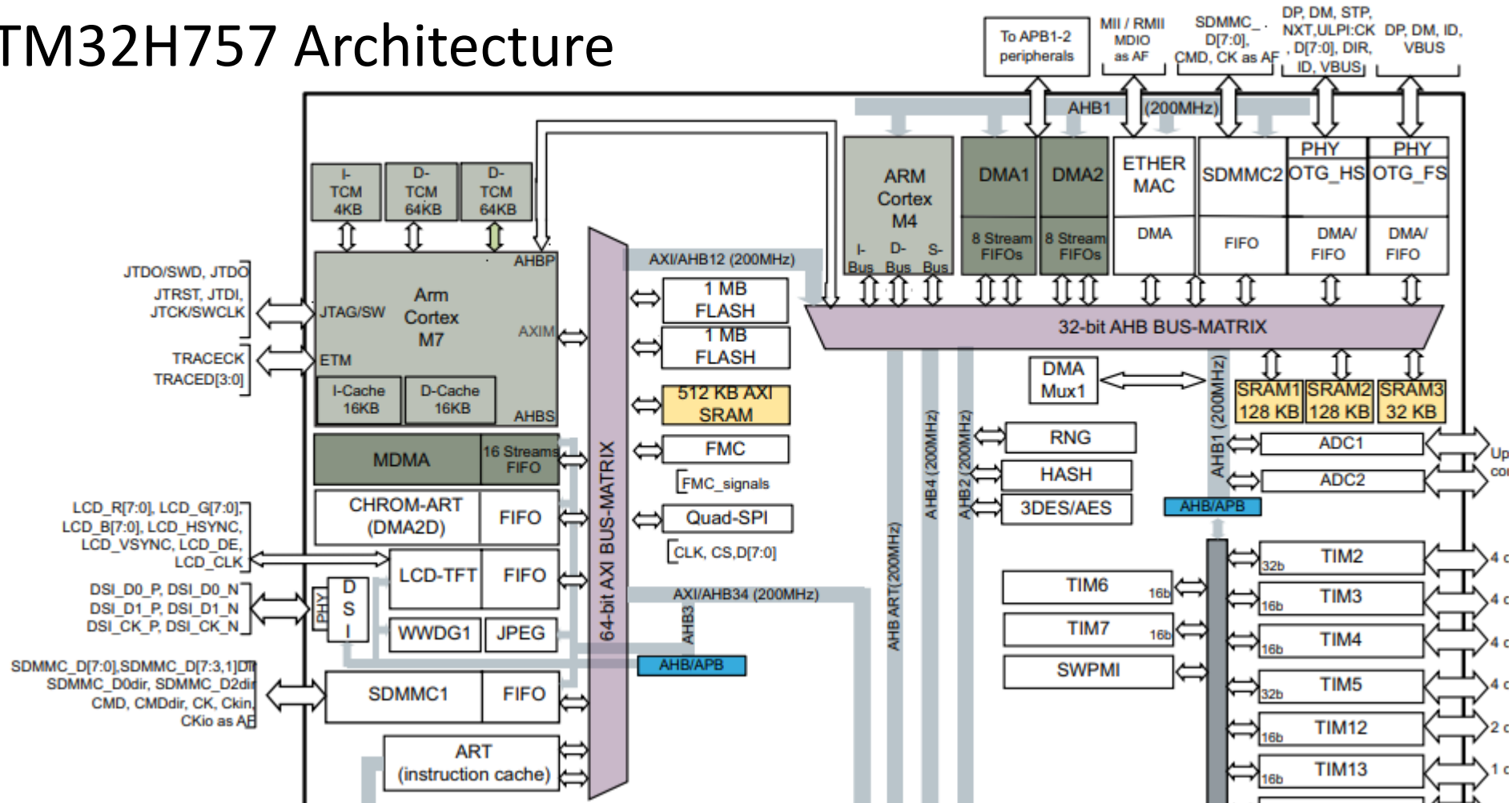
The STM32 Cortex-M4 Implementation



The STM32 Cortex-M7 Implementation



The STM32H757 Architecture



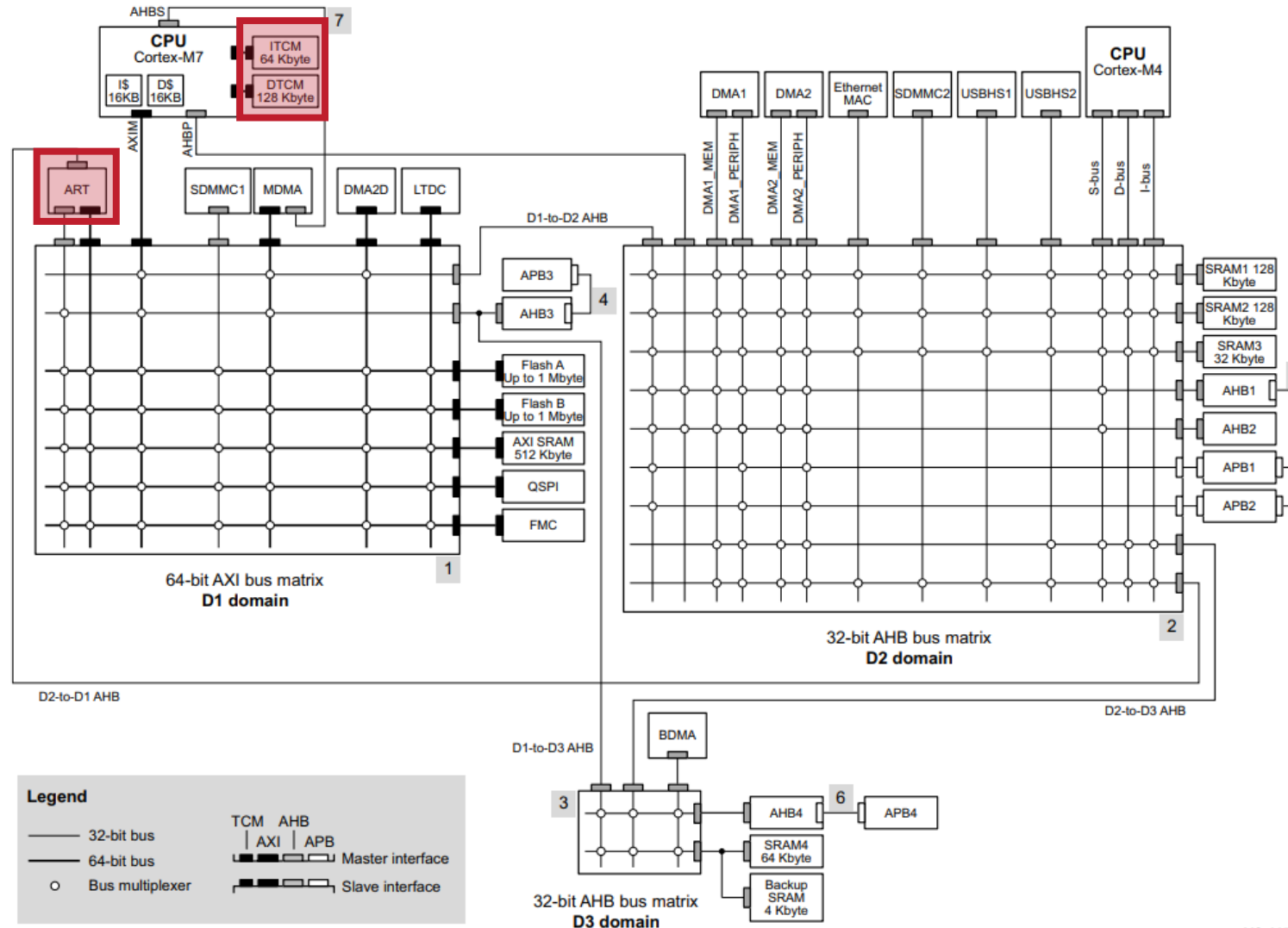


Table 2. Bus-master-to-bus-slave interconnect

Bus slave / type ⁽¹⁾	Bus master / type ⁽¹⁾																				
	Cortex-M7 - AXIM	Cortex-M7 - AHBP	Cortex-M7 - ITCM	Cortex-M7 - DTCM	SDMMC1	MDMA	MDMA - AHBS	DMA2D	LTDC	DMA1 - MEM	DMA1 - PERIPH	DMA2 - MEM	DMA2 - PERIPH	Eth. MAC - AHB	SDMMC2 - AHB	USBHS1 - AHB	USBHS2 - AHB	Cortex-M4 - S-bus	Cortex-M4 - D-bus	Cortex-M4 - I-bus	BDMA - AHB
ITCM	-	-	X	-	-	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-
DTCM	-	-	-	X	-	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-
AHB3 periph	X	-	-	-	-	X	-	-	-	X	X	X	X	X	X	X	X	X	X	X	-
APB3 periph	X	-	-	-	-	X	-	-	-	X	X	X	X	X	X	X	X	X	X	X	-
Flash bank 1	X	-	-	-	X	X	-	X	X	X	X	X	X	X	X	X	X	X	X	X	-
Flash bank 2	X	-	-	-	X	X	-	X	X	X	X	X	X	X	X	X	X	X	X	X	-
AXI SRAM	X	-	-	-	X	X	-	X	X	X	X	X	X	X	X	X	X	X	X	X	-
QUADSPI	X	-	-	-	X	X	-	X	X	X	X	X	X	X	X	X	X	X	X	X	-
FMC	X	-	-	-	X	X	-	X	X	X	X	X	X	X	X	X	X	X	X	X	-
SRAM 1	X	-	-	-	-	X	-	X	-	X	X	X	X	X	X	X	X	X	X	X	-
SRAM 2	X	-	-	-	-	X	-	X	-	X	X	X	X	X	X	X	X	X	X	X	-
SRAM 3	X	-	-	-	-	X	-	X	-	X	X	X	X	X	X	X	X	X	X	X	-
AHB1 periph	-	X	-	-	-	X	-	X	-	X	X	X	X	-	-	-	-	X	-	-	-
APB1 periph	-	X	-	-	-	X	-	X	-	X	X	X	X	-	-	-	-	X	-	-	-
AHB2 periph	-	X	-	-	-	X	-	X	-	X	X	X	X	-	-	-	-	X	-	-	-
APB2 periph	-	X	-	-	-	X	-	X	-	X	X	X	X	-	-	-	-	X	-	-	-
AHB4 periph	X	-	-	-	-	X	-	-	-	X	X	X	X	X	X	X	X	X	-	-	X
APB4 periph	X	-	-	-	-	X	-	-	-	X	X	X	X	X	X	X	X	X	-	-	X
SRAM4	X	-	-	-	-	X	-	-	-	X	X	X	X	X	X	X	X	X	-	-	X
Backup RAM	X	-	-	-	-	X	-	-	-	X	X	X	X	X	X	X	X	X	-	-	X

1. **Bold** font type denotes 64-bit bus, plain type denotes 32-bit bus.
 2. "X" = access possible, "-" = access not possible, shading = access useful/usable.

A few useful definitions

ART accelerator – adaptive real-time memory access accelerator

ITCM-RAM – instruction trace ram can be accessed at maximum CPU clock without latency. Located on the Cortex-M7 at 0x0000 0000.

Which domain contains shared memory between the two cores?

- D1 Domain (High-Performance block)
- D2 Domain (Communication peripherals and timers)
- D3 Domain (reset/clock control/power management)

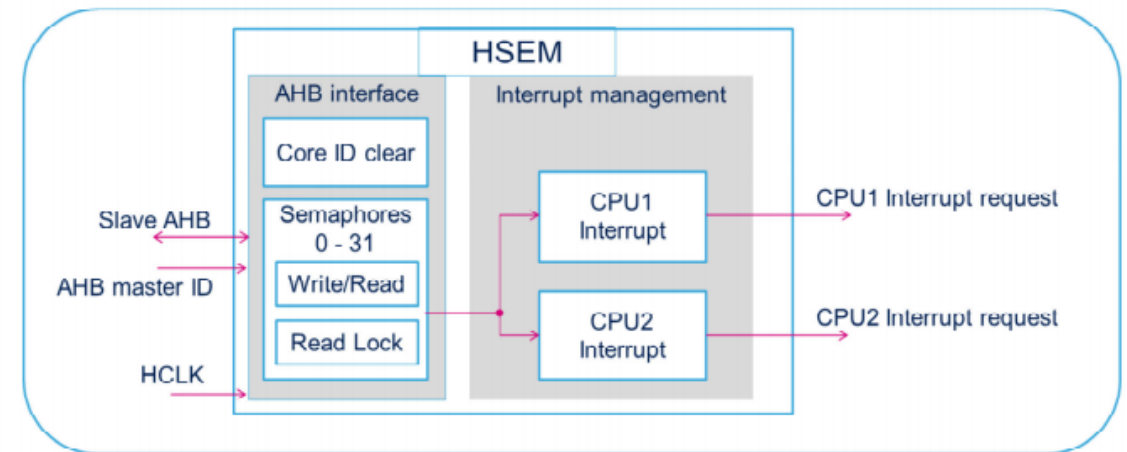
Processor Boot Options

- Simultaneous Boot (CM4 and CM7)
- Boot CM4 (CM7 Gated)
- Boot CM7 (CM4 Gated)

The HSEM Peripheral

HSEM is a hardware semaphore module used to manage access permissions and synchronization of resources between multiple processes.

- 32 Semaphores
- Multiple locking mechanisms
 - 1 step read lock
 - 2 step write, read back lock
- Located on the AHB interface bus



Source: STM

What are some possible applications for the HSEM?

- Used prior to a peripheral access
- Manage shared resources
- Synchronize processes
- All the above
- None of the above

Thank you for attending

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