

Industrial Ethernet Designs with MCUs- a Hands on Introduction

Class 5: Industrial Ethernet Examples

12/15/2017

Warren Miller

This Week's Agenda

- 12/11/17 An Overview of Ethernet
- 12/12/17 An Introduction to Industrial Ethernet
- 12/13/17 Industrial Ethernet Applications
- 12/14/17 Industrial Ethernet Implementations
- 12/15/17 Industrial Ethernet- examples

Course Description

- Industrial Ethernet is still a key communication technology for factory control.
- It is built on the long legacy of Ethernet, but adds significant capabilities for increasing robustness and reliability.
- This course will provide an overview of the key differences between our familiar Ethernet protocol and the Industrial version.
- A hands on example will use easily available software and development boards to dig into some of the key details of an actual Industrial Ethernet implementation. Students can optionally obtain the hardware and software to follow along with the implementation.

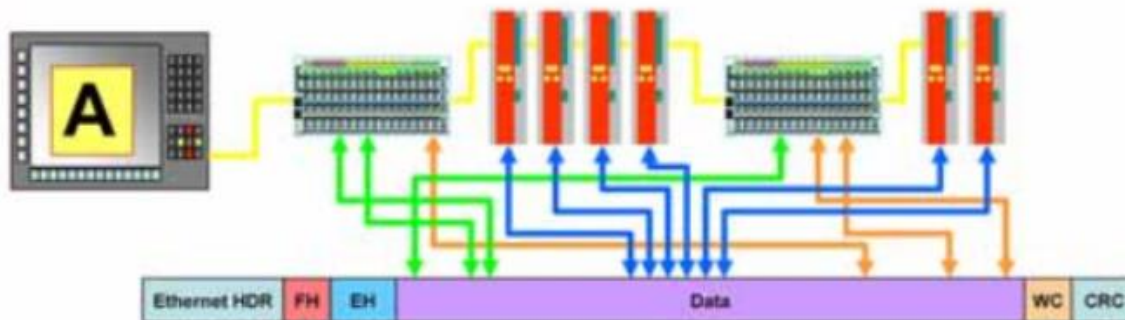
Today's Topics

This class will provide an example implementation using one of the target platforms described in the previous class and the focus of the design resources will be based on input from the students during the first two classes.

- Industrial Ethernet in real applications
- A robust reference design- TI AMIC110 and Concerto C2000
- Other reference platforms

EtherCAT Overview

- EtherCAT is:
 - Industrial Ethernet down to the I/O Level
 - Flexible Wiring and simple Configuration
 - Lower cost, Well proven, An Open technology
- Key Principle: Frame processing on the fly
- Master used standard Ethernet controllers

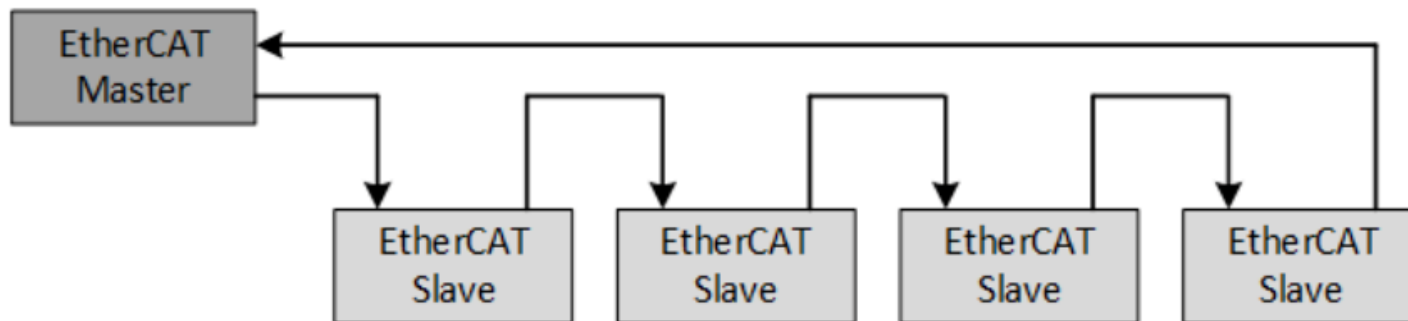


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Industrial Ethernet Technologies

Typical EtherCAT Network

EtherCAT has exactly one master node per network. The master can be implemented on a standard Ethernet media access controller (MAC) without an additional communication processor. This MAC has to provide a full-duplex 100 Mbit/s interface. The figure below shows a daisy-chain network EtherCAT can also be implemented in a line, tree, or star configuration.

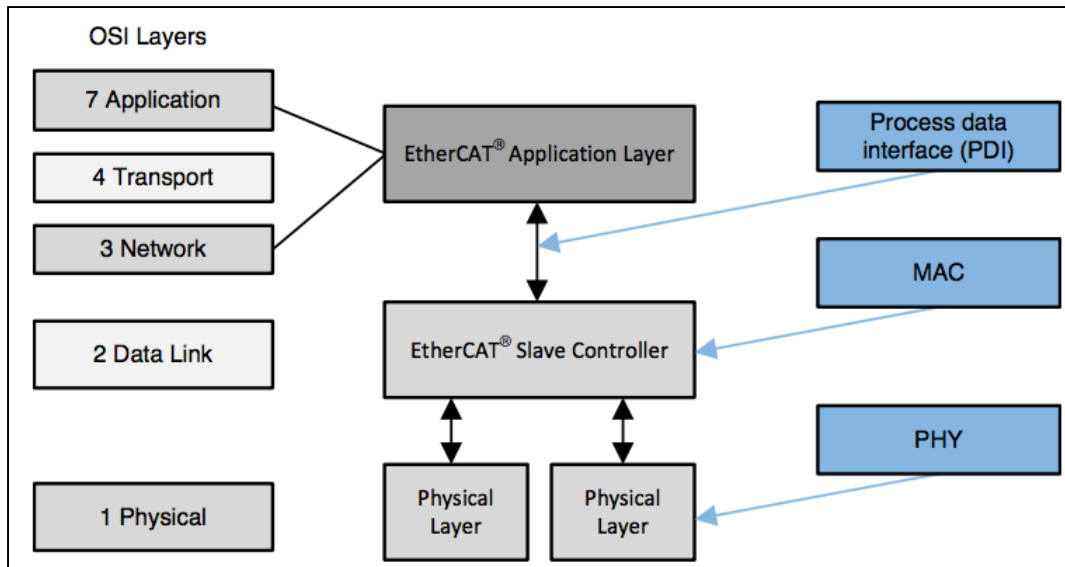


Contrary to the operation of standard Ethernet, the EtherCAT slave processes the EtherCAT frames on the fly. This means that the transmission of the new EtherCAT packet starts as soon as possible before completely receiving the incoming data packet.

Typical EtherCAT Network

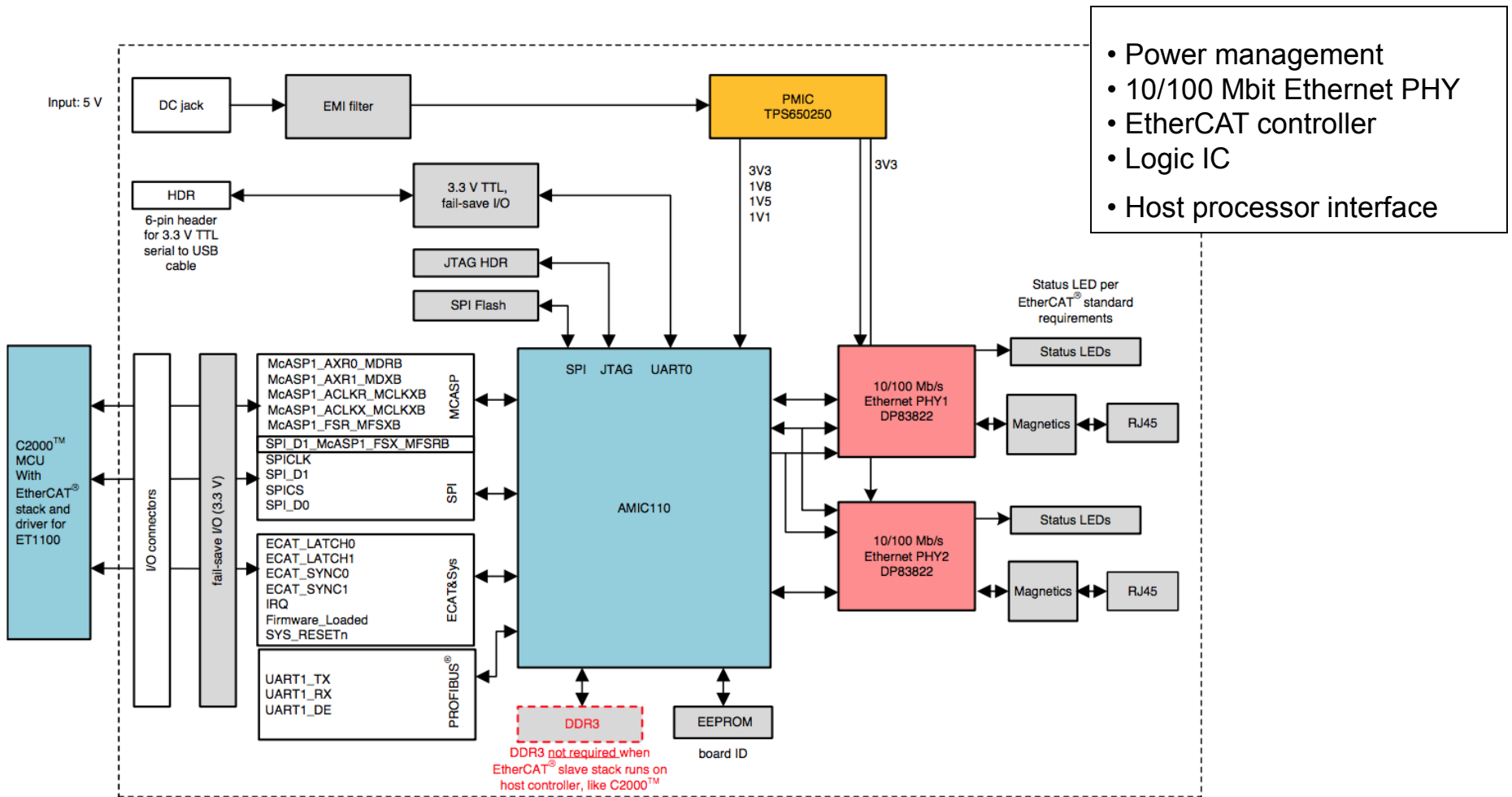
Physical Layer: 100BASE-TX copper, 100BASE-FX optical fiber, or E-bus (Ethernet-Klemmenbus) based on LVDS signaling as a transmit medium.

EtherCAT MAC Layer: The MAC layer is implemented according to the EtherCAT standard specification IEC61158. The implementation has to support the standard TCP-IP and UDP-IP protocols besides handling the EtherCAT data frames.



Application Layer: Different process data interfaces (PDI) are available, depending on the chosen ESC. Typical interface options vary from 32-bit to 8- or 16-bit parallel IO interfaces or serial interfaces like SPI. In the application layer the EtherCAT slave processes data or executes various functions, which are defined in specific profiles.

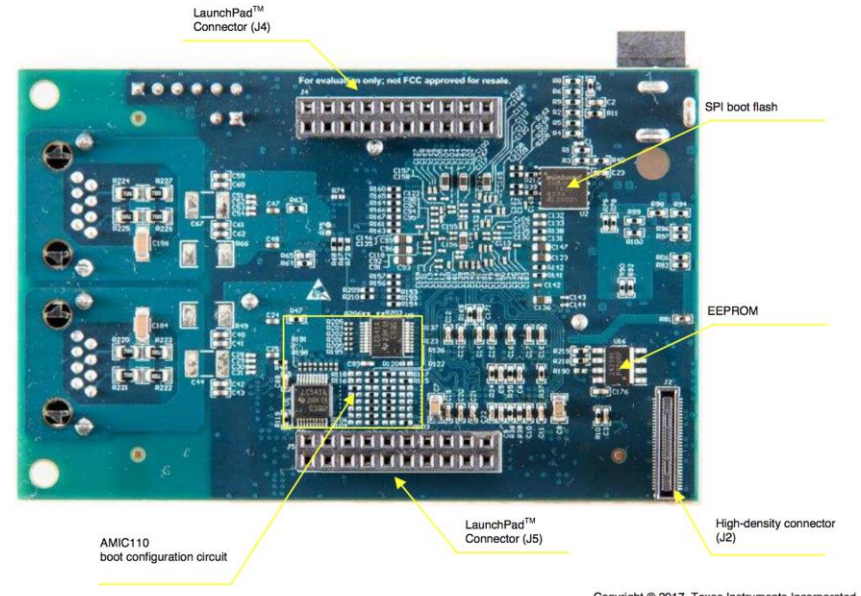
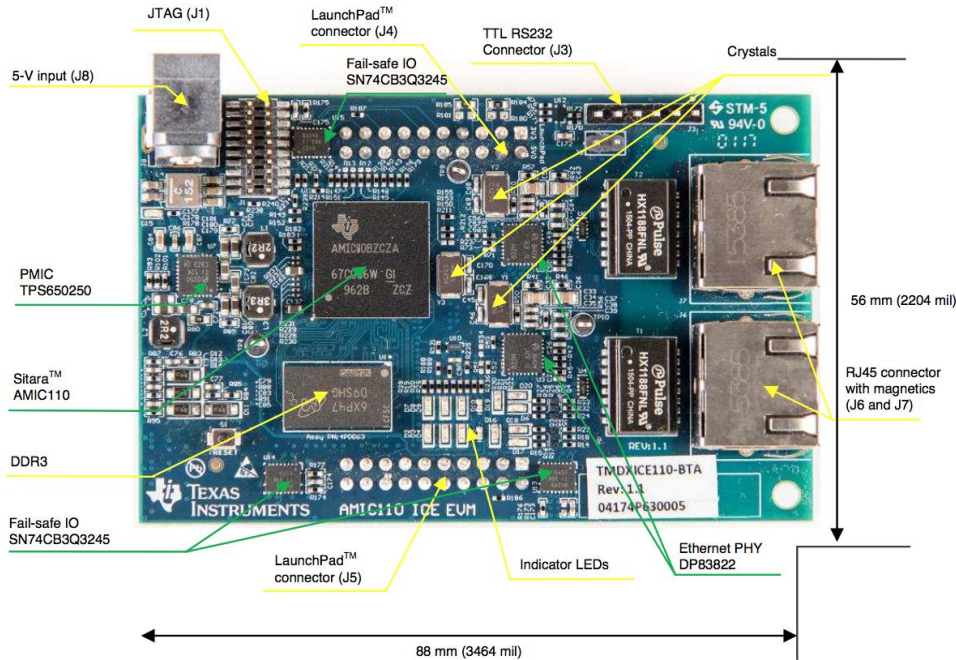
Design Block Diagram



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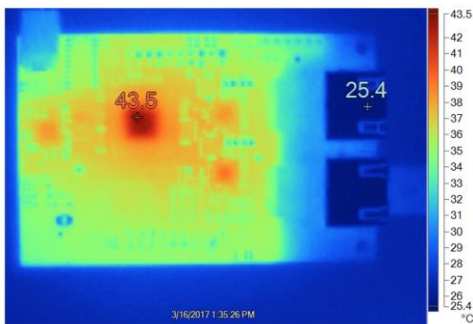
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Reference Design Board



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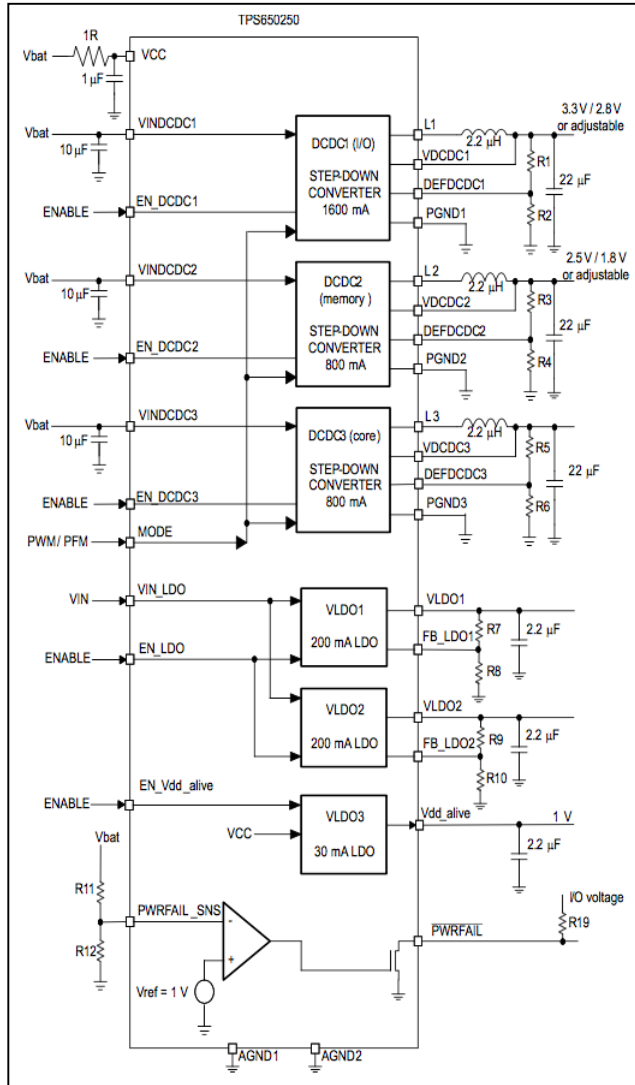
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| RAIL | TPS650250 MAXIMUM OUTPUT CURRENT | TECHNOLOGY | CURRENT CONSUMPTION | POWER CONSUMPTION |
|-------|----------------------------------|------------|---------------------|-------------------|
| 1.1 V | 1600 mA | SMPS | 349 mA | 0.384 W |
| 1.5 V | 800 mA | SMPS | 35.8 mA | 0.054 W |
| 1.8 V | 400 mA | LDO | 26.23 mA | 0.047 W |
| 3.3 V | 800 mA | SMPS | 128 mA | 0.422 W |

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Design: Power Management



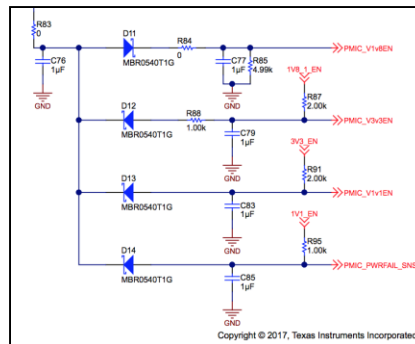
| VOLTAGE OPTION | PARAMETER | VOLTAGE | MAXIMUM POWER CONSUMPTION | COMMENT |
|----------------|---------------|---------|---------------------------|---|
| One | IO supply | 3.3 V | 261 mW | Choose voltage depending on power budget on different rails |
| | Analog supply | 3.3 V | | |
| Two | IO supply | 1.8 V | 126 mW | Choose voltage depending on power budget on different rails |
| | Analog supply | 1.8 V | | |

| RAIL | SITARA | DDR3 |
|----------------------|---------|---------|
| 1.1 V | ~420 mA | — |
| 1.5 V ⁽¹⁾ | ~120 mA | ~140 mA |
| 1.8 V | ~33 mA | — |
| 3.3 V | ~34 mA | — |

⁽¹⁾ is DDR3 interface using 1.5 V

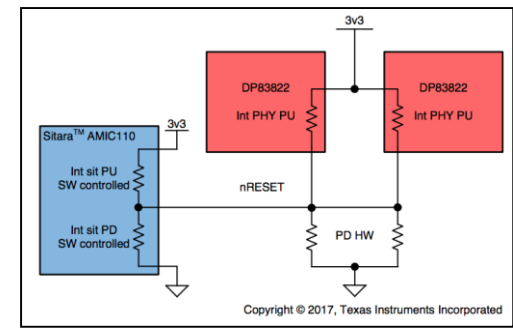
| RAIL | FLASH | GLUE LOGIC | LEDS | DRIVING IO |
|-------|--------|------------|--------|------------|
| 3.3 V | ~25 mA | ~10 mA | ~16 mA | ~83 mA |

| RAIL | AMIC110 | DDR3 | SINGLE SUPPLY DP83822 | EXTERNAL CIRCUIT |
|----------------------|---------|---------|-----------------------|------------------|
| 1.1 V | ~420 mA | — | — | — |
| 1.5 V ⁽¹⁾ | ~120 mA | ~140 mA | — | — |
| 1.8 V | ~33 mA | — | — | — |
| 3.3 V | ~34 mA | — | ~159 mA | ~138 mA |

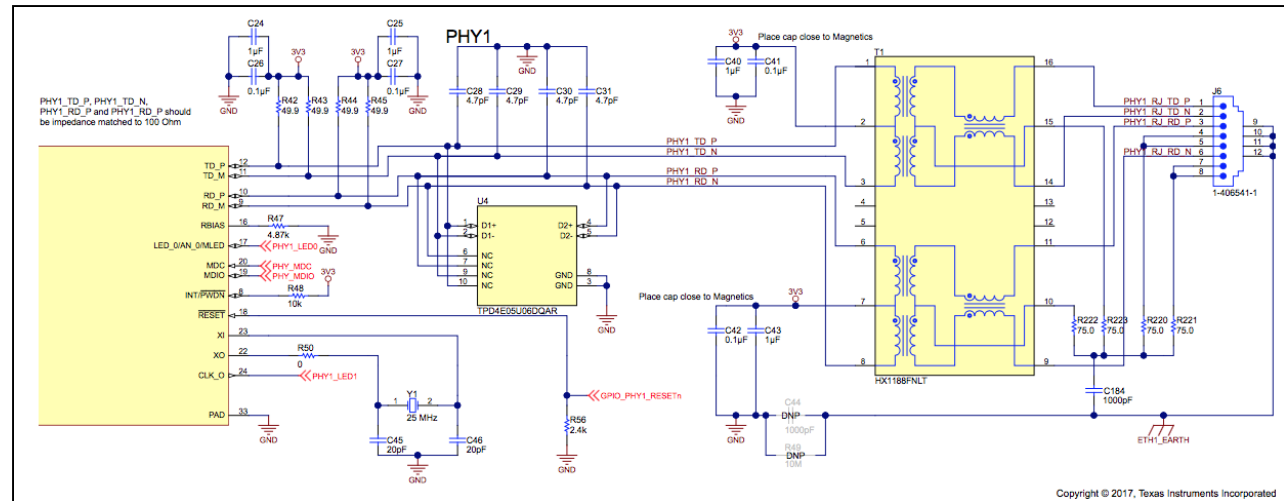
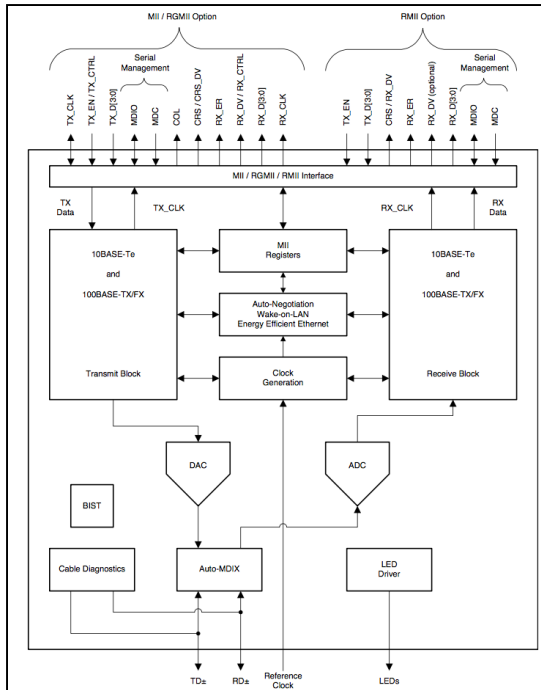


Design: PHY

- Reset Circuitry
- Interface- MII
- Interface PHY to Jack

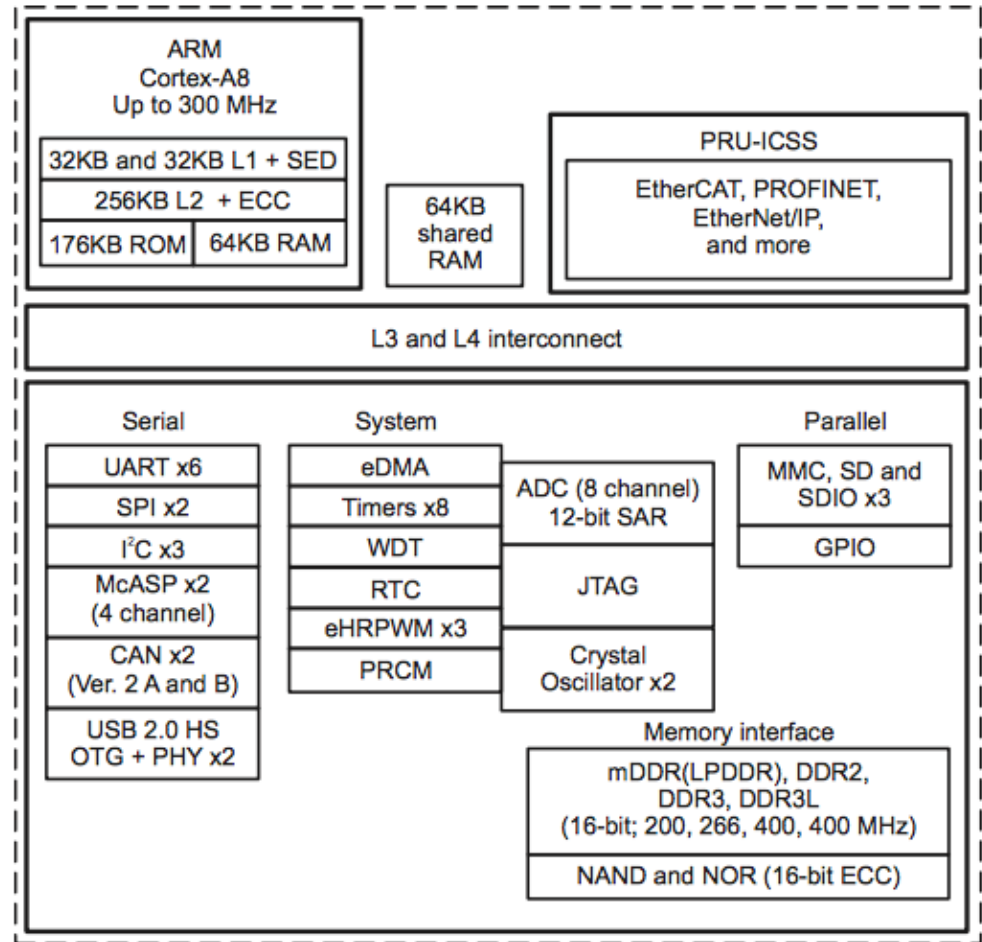


| DESCRIPTION | NET NAME | PINS |
|--------------------|------------|------|
| Transmit clock | PHYx_TXCLK | 1 |
| Transmit data | PHYx_TXDn | 4 |
| Transmit enable | PHYx_TXEN | 1 |
| Receive clock | PHYx_RXCLK | 1 |
| Receive data | PHYx_RXDn | 4 |
| Receive error | PHYx_RXER | 1 |
| Receive data valid | PHYx_RXDV | 1 |
| Collision detect | PHYx_COL | 1 |
| Carrier sense | PHYx_CRS | 1 |
| Total | — | 15 |



AMIC110 Processor

- ARM Cortex-A8
- L1 and L2 cache
- ROM and RAM
- Shared RAM
- PRU-ICSS
- Programmable Real-Time Unit Subsystem and Industrial Communications Subsystem
- Peripherals



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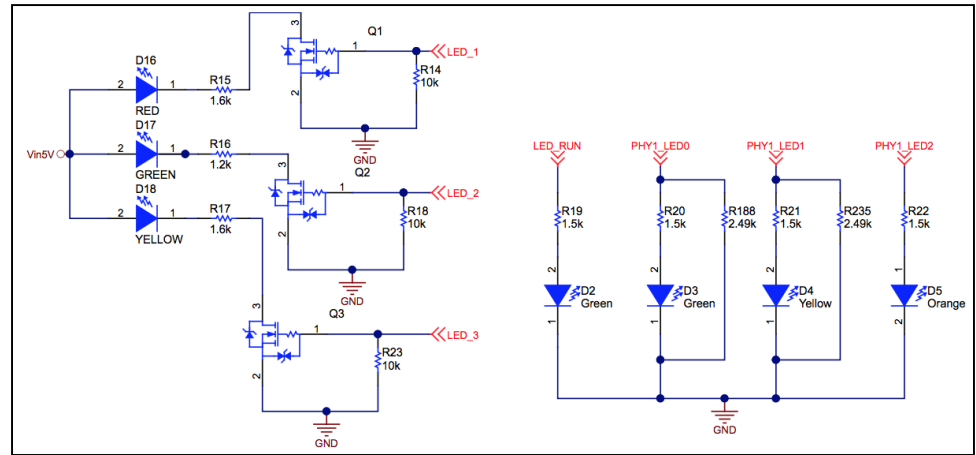
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Design: AMIC110 Memory I/O

- **DDR3:** Because only one DDR3 memory chip is necessary, the termination of the DDR3 data lines can be neglected if the layout is done correctly. The characteristic impedance of each trace must match that of the DDR3 IC.
- **SPI Flash:** The flash chip was chosen to have a cost-optimized boot option. The boot configuration pins of the AMIC110 are set so that it will boot from the SPI flash.
- **I2C EEPROM:** The EEPROM memory is used for board identification purposes. The Ethernet MAC addresses can also be stored there.

Design: AMIC110 Peripheral I/O

- LEDs
- Pins during Boot
- Unused circuits
- SPI, UART0/1, GPIO, EtherCAT, Host I/F



| GROUP | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|-----------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| ZCZ BALL NUMBER | B6 | C7 | B7 | A7 | C8 | B8 | A8 | C9 | C18 | B18 | C17 | C16 | R6 |
| PD OR PU OR Z | Z | Z | Z | Z | Z | Z | Z | Z | PD | PU | PU | PU | PD |
| ZCZ BALL NUMBER | R1 | R2 | R3 | R4 | T1 | T2 | T3 | T4 | U1 | U2 | U3 | U4 | V2 |
| PD OR PU OR Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z | Z |
| ZCZ BALL NUMBER | V3 | V4 | T5 | R5 | V5 | U5 | B15 | B4 | B5 | D14 | A17 | A16 | C15 |
| PD OR PU OR Z | Z | Z | Z | PD | PD | PD | Z | Z | Z | PD | PU | PU | PU |
| ZCZ BALL NUMBER | B17 | B16 | E16 | E18 | E15 | E17 | D15 | D16 | D17 | D18 | A9 | B9 | A15 |
| PD OR PU OR Z | PU | PU | PU | PU | PU | PU | PU | PU | PU | PU | Z | Z | PD |

Table 15. Disabling AMIC110's Real-time Clock Subsystem

| PIN | CONNECT TO |
|---------------|----------------|
| VDDS_RTC | 1.8V |
| CAP_VDD_RTC | 1.1V(VDD_CORE) |
| RTC_KALDO_ENn | 1.8V(VDDS_RTC) |
| RTC_PWRONRSTn | GND(VSS) |
| PMIC_POWER_EN | NC |
| EXT_WAKEUP | GND(VSS) |
| RTC_XTAL | NC |
| VSS_RTC | GND(VSS) |

Table 16. Disabling AMIC110's USB Interface

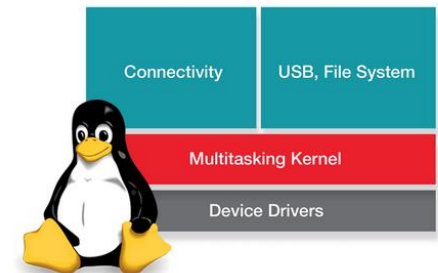
| PIN | CONNECT TO |
|--------------|-------------|
| VDDA1P8V_USB | 1.8V |
| VDDA3P3V_USB | 3.3V or GND |
| VSSA_USB | GND |
| USBx_DP | NC or GND |
| USBx_DM | NC or GND |
| USBx_CE | NC |
| USBx_ID | NC or GND |
| USBx_DRVVBUS | NC |
| USBx_VBUS | NC or GND |

Presented by:

Accessing the Software Platform






Download Software

- The TI Processor SDK is a unified software platform for TI's newest Processor families.
- Features scalable Linux, TI-RTOS and Android support
- Includes complete board support packages, documentation, libraries, benchmarks, utilities, and code examples
- Allows you to seamlessly reuse and migrate software across TI processor families
- Maintained and released on a quarterly basis
- Downloadable from TI's website, free of charge
- Supported by TI's E2E forums
- Benefits from the ongoing TI contributions, via up-streamed patches, to Mainline Linux





Reference Design Software

- The Processor SDK for AMIC110 comes with the bootloader (MLO).
- To program the onboard SPI memory, the SDK comes with a flash tool, which can also be found in this package.
- The bootloader has to be configured to boot from SPI flash. This configuration can be completed by picking the correct build option.
- A user guide, the EtherCAT libraries, prebuilt binaries, and example source code can be found at: [PRU-ICSS-ETHERCAT-SLAVE](#)

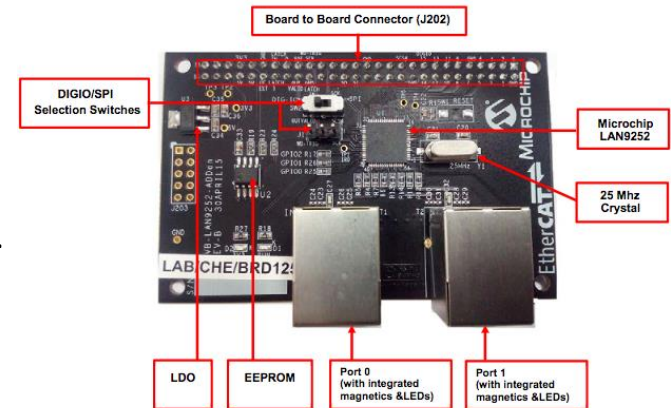
| Title | Description | Size |
|---|--|-------|
| PRU-ICSS EtherCAT Slave 01.00.04.02 | | |
|  PRU-ICSS EtherCAT Slave Linux Installer | EtherCAT Slave package | 5988K |
|  PRU-ICSS EtherCAT Slave Windows Installer | EtherCAT Slave package | 7812K |
|  Prebuilt binaries | PRU-ICSS EtherCAT Slave pre-built binaries | 552K |
| Industrial Protocol Packages Software Developers Guide | Software Developers Guide | |
| Industrial Protocol Packages Getting Started Guide | Getting Started Guide | |
| PRU-ICSS EtherCAT Slave User Guide | User Guide | |
| PRU-ICSS EtherCAT Slave Release Notes | Release Notes | |
|  Software Manifest | Software Manifest of the components in the package | 24K |
|  Firmware Datasheet | Firmware Datasheet | 556K |
| Processor SDK RTOS documentation | | |
| Processor SDK RTOS documentation | Developers guide for Processor SDK RTOS | |
| AM335x EVM Documentation | | |
| AM335x Industrial Communications Engine Quick Start Guide | Quick Start Guide included in the EVM kit | |
| AM437x EVM Documentation | | |
| AM437x Industrial Development Kit Quick Start Guide | Quick Start Guide included in the EVM kit | |
| AM57xx IDK Documentation | | |
| AM572x IDK Quick Start Guide | Quick Start Guide that was included in the EVM kit | |
| AM571x IDK Quick Start Guide | Quick Start Guide that was included in the EVM kit | |
| PRU-ICSS-EtherCAT_Slave Checksums | | |
| md5sum_ethercat_slave.txt | MD5 Checksums for EtherCAT Slave package | 4K |

Legend

-  Fill in Form. Approved users receive download URL in 1 minute.
-  Fill in Form. TI will contact you in 1-2+ business days.

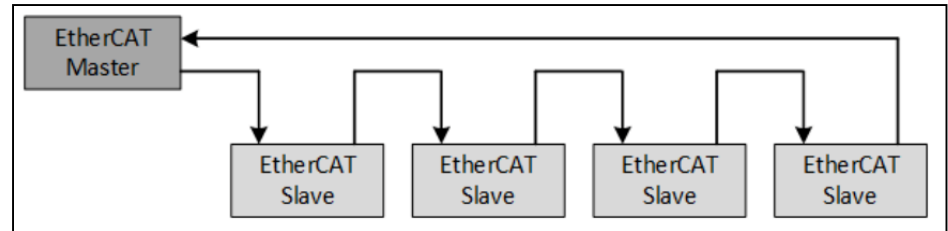
Other Reference Designs

- The NXP QorIQ® communications processors include single-, dual-, quad- and multicore processor architectures with integrated support for communications protocols such as EtherCAT. [Fact Sheet](#) [Order at Digi-Key](#)
- The Microchip LAN9252 is a 2-port EtherCAT Slave Controller (ESC) with dual-integrated Ether-net PHYs which each contain a full-duplex 100BASE-TX transceiver and support 100Mbps (100BASE-TX) operation. 100BASE-FX is supported via an external fiber transceiver. [Fact Sheet](#) [Order at Digi-Key](#)

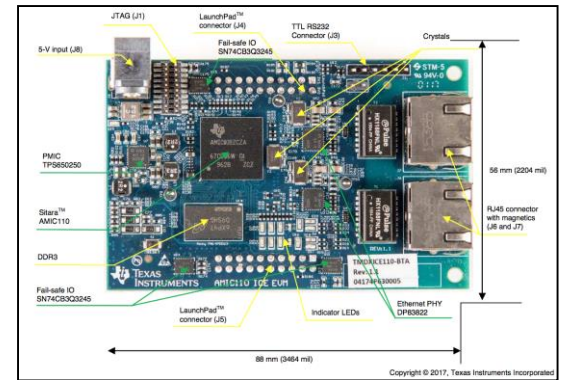


Conclusion

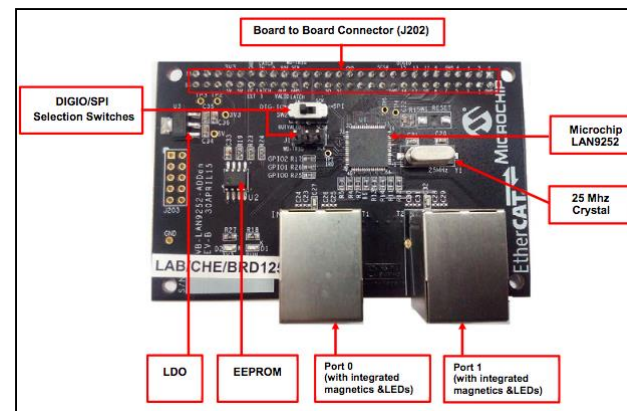
EtherCAT Refresher



EtherCAT Implementation



Other Reference Designs



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Class Resources

TI Industrial Control with Concerto MCU

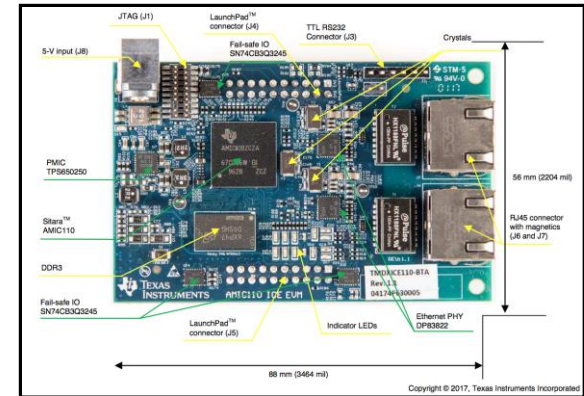
- https://dkc1.digikey.com/IE/en/TOD/Texas_Instruments/Connectivity-Control-Systems/Connectivity-Control-Systems.html

AMIC110 Platform

- <http://www.ti.com/lit/ug/tidud02/tidud02.pdf>
- http://processors.wiki.ti.com/index.php/PRU_ICSS_EtherCAT

Other Platforms

- NXP [Order at Digi-Key](#)
- Microchip [Order at Digi-Key](#)



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| Industrial Protocol Packages Software Developers Guide | Software Developers Guide | |
| Industrial Protocol Packages Getting Started Guide | Getting Started Guide | |
| PRU-ICSS EtherCAT Slave User Guide | User Guide | |
| PRU-ICSS EtherCAT Slave Release Notes | Release Notes | |
| Software Manifest | Software Manifest of the components in the package | 24K |
| Firmware Datasheet | Firmware Datasheet | 556K |
| Processor SDK RTOS documentation | | |
| Processor SDK RTOS documentation | Developers guide for Processor SDK RTOS | |
| AM335x EVM Documentation | | |
| AM335x Industrial Communications Engine Quick Start Guide | Quick Start Guide included in the EVM kit | |
| AM437x EVM Documentation | | |
| AM437x Industrial Development Kit Quick Start Guide | Quick Start Guide included in the EVM kit | |
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| m5Sum_ethercat_slave.txt | MDS Checksums for EtherCAT Slave package | 4K |

Legend
 ZIP in Form: Approved users receive download URL, in 1 minute.
 PDF in Form: It will contact you in 1-2 business days.

Course Resources

Industrial Ethernet Overview- TI

- <http://www.ti.com/lit/wp/spry254/spry254.pdf>

Industrial Communications Kit

- <https://www.digikey.com/en/product-highlight/t/texas-instruments/industrial-communications-engine-using-tis-am3359>

EtherCAT Article

- <https://www.digikey.com/en/articles/techzone/2015/aug/mcus-and-ethercat-gear-up-for-the-industrial-internet-of-things>

Connectivity and Control Systems- TI

- https://dkc1.digikey.com/IE/en/TOD/Texas_Instruments/Connectivity-Control-Systems/Connectivity-Control-Systems.html

Embedded Ethernet- MicroChip

- <https://dkc1.digikey.com/IE/en/TOD/microchip/EmbeddedEthernet/EmbeddedEthernet.html>

- https://dkc1.digikey.com/IE/en/TOD/Microchip/Ethernet_Controller_Solution/Ethernet_Controller_Solution.html

Introduction to Industrial Ethernet

- http://www.bb-elec.com/Learning-Center/All-White-Papers/Ethernet/Introduction-to-Industrial-Ethernet/AnIntroductionToIndustrialEthernet-WP12B-R1_1112.pdf

Additional Resources

- <http://www.ti.com/lit/wp/spry254/spry254.pdf>
- https://www.ethercat.org/download/documents/Industrial_Ethernet_Technologies.pdf
- https://www.youtube.com/watch?v=gphJtw0pluo&list=PLgUXqPkOStPum60jqifNt7IDY9_0a0_rX&index=14

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