Designing and Launching an Embedded Product

Class 4: Achieving Quality and Reasonable Time-to-Market

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Presented by:

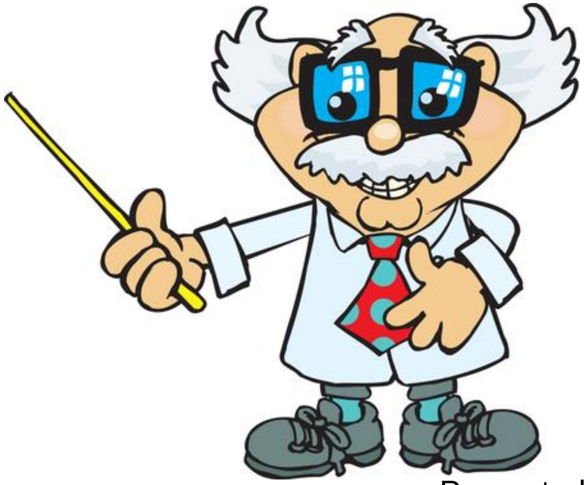
Course Overview

Topics:

- The Business of Product Development
- Success through Design and Development Processes
- Scalability, Architectures and the MVP
- **Achieving Quality and Reasonable Time to Market**
- Techniques for Accelerating Time to Market

Session Overview

- Balancing Development
- Software Quality
- Managing Quality



Balancing Development

Balancing Development

Example Inputs:

Quality – High

Time – Short

Results:

Cost - High

Software Quality

Quality is completely subjective

- How does FatFS rank?
- How does FreeRTOS rank?
- How does silicon vendor code rank?
- Commercial code?

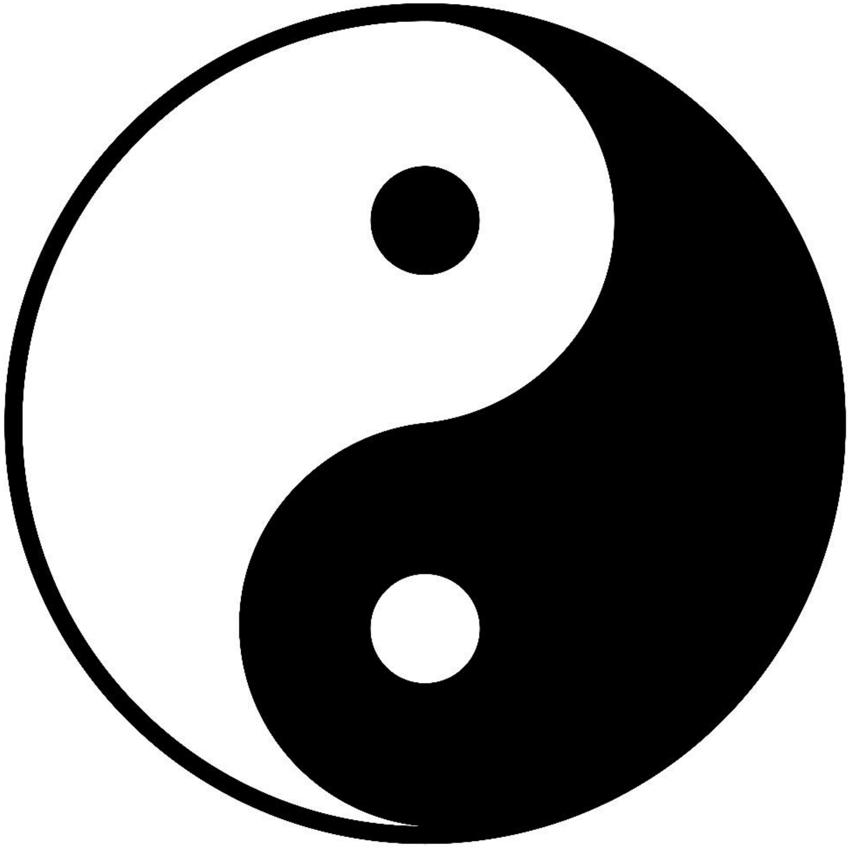
Software Quality

Define what quality is to you:

- Adhering to Industry Best Practices
- Minimizing Cyclomatic Complexity
- Compilation with No Warnings
- Code Testing Coverage
- Code Verification

Software Quality

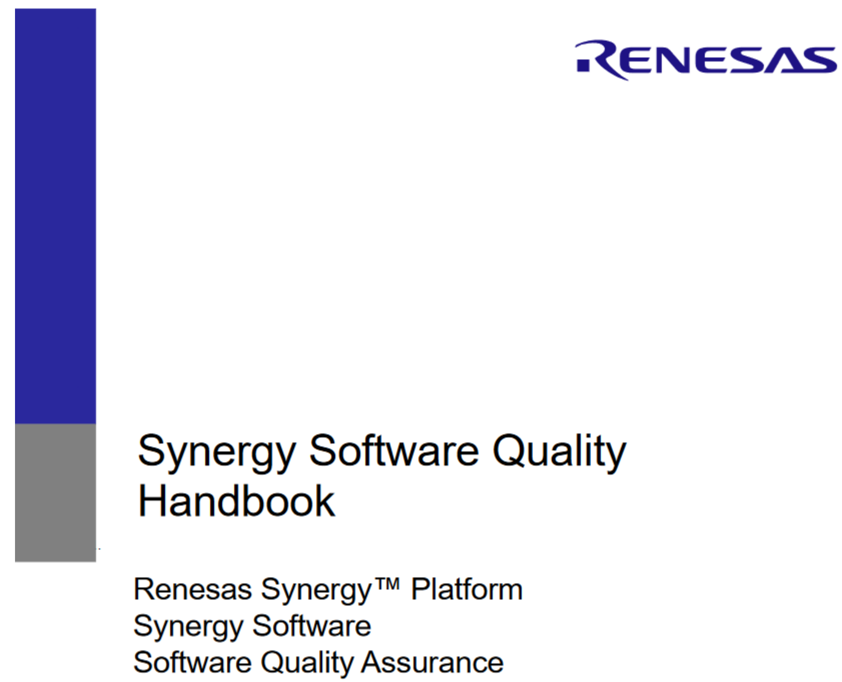
Software Quality Assurance (SQA)



Software Development Life Cycle (SLDC)

Software Quality

- Definitions
- SDLC Activities
- Documentation
- Standards and Conventions
- Maintenance
- Software Metrics
- Verification


RENESAS

Synergy Software Quality Handbook

Renesas Synergy™ Platform
Synergy Software
Software Quality Assurance

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Cyclomatic Complexity

Cyclomatic Complexity (McCabe Complexity) defines the number of linearly independent paths in a function of code.

```
                    ~~ File Functional Summary ~~

File Function Count.....:          5
Total Function LOC.....:          35   Total Function Pts LOC :        0.5
Total Function eLOC....:          17   Total Function Pts eLOC:        0.3
Total Function lLOC....:          14   Total Function Pts lLOC:        0.2
Total Function Params .:           7   Total Function Return .:          5
Total Cyclo Complexity :           8   Total Function Complex.:         20
       ------     -----     -----     ------     ------     -----
Max Function LOC ......:          21   Average Function LOC ..:       7.00
Max Function eLOC .....:          11   Average Function eLOC .:       3.40
Max Function lLOC .....:           8   Average Function lLOC .:       2.80
       ------     -----     -----     ------     ------     -----
Max Function Parameters:           2   Avg Function Parameters:       1.40
Max Function Returns ..:           1   Avg Function Returns ..:       1.00
Max Interface Complex. :           3   Avg Interface Complex. :       2.40
Max Cyclomatic Complex.:           4   Avg Cyclomatic Complex.:       1.60
Max Total Complexity ..:           6   Avg Total Complexity ..:       4.00
________________________________________________________________________
End of File: C:\SPO2 Module\Common\drivers\src\pwm.c
```


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Cyclomatic Complexity

Higher code complexity increases debugging effort and decreases code reliability

Complexity	Reliability Risk
1 – 10	A simple function, little risk
11 – 20	More complex moderate risk
21 - 50	Complex, high risk
51+	Untestable, very high risk

Higher code complexity increases risk of injecting new bugs into code!

Complexity	Risk of injecting a bug when making a change
1 – 10	5%
11 – 20	20%
21 - 50	40%
51+	60%

DesignNews
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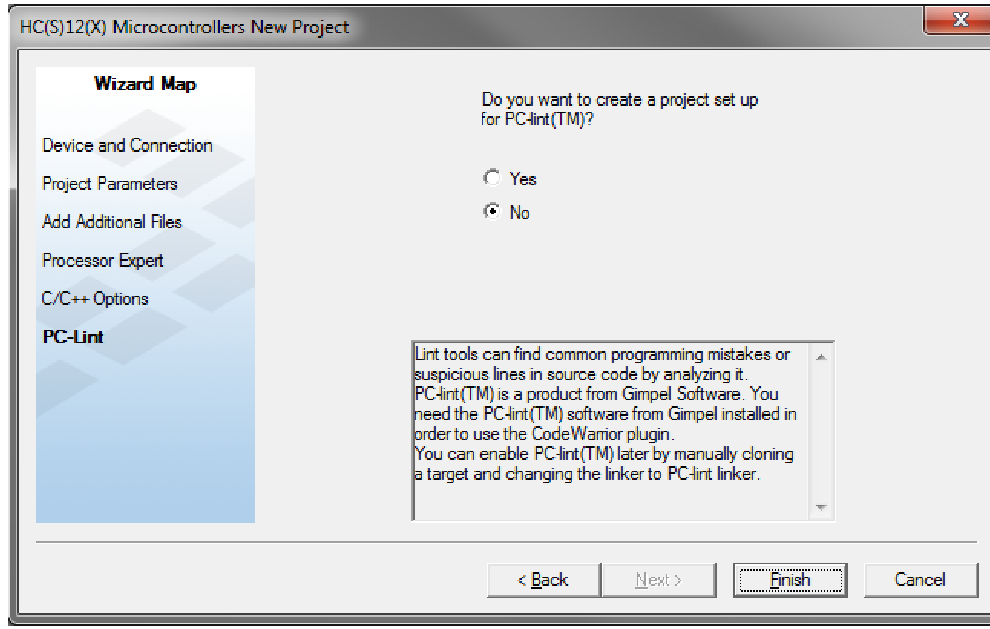
Digi-Key ELECTRONICS

Code Analysis

Ways to Perform Code Analysis

- Complexity Measurements
- Lines of Code
- Comment Density
- Assertion Density
- Static Code Analysis
- Dynamic Code Analysis
- Worst Case Stack Usage
- Automated Tools
  - (i.e. Code Standard Compliance)



Automated Tests

Benefits:

- Simplify regression testing
- Run tests on build server
- Easily identify when a test fails (and what caused it)
- Monitor code coverage
- Automated reporting

Test Harnesses

```
TEST(DRV_TIMER_TG1, TC_1_1_OpenSuccess) PASS
TEST(DRV_TIMER_TG1, TC_1_2_OpenHdl) PASS
TEST(DRV_TIMER_TG1, TC_1_3_OpenCallbackParameter) PASS
TEST(DRV_TIMER_TG1, TC_1_4_OpenConfigIsNull) PASS
TEST(DRV_TIMER_TG1, TC_1_5_OpenConfigChannelOutOfRange) PASS
TEST(DRV_TIMER_TG1, TC_1_6_OpenOneShot) PASS
TEST(DRV_TIMER_TG1, TC_1_10_OpenTwice) PASS
TEST(DRV_TIMER_TG1, TC_1_11_OpenCallbackIRQNotAvailable) PASS
TEST(DRV_TIMER_TG1, TC_1_12_OpenPeriodTooLarge) PASS
TEST(DRV_TIMER_TG1, TC_1_13_MultipleChannels) PASS
TEST(DRV_TIMER_TG2, TC_2_1_NullPointers) PASS
TEST(DRV_TIMER_TG2, TC_2_2_StartStopClear) PASS
TEST(DRV_TIMER_TG2, TC_2_3_SetGetDelay) PASS
TEST(DRV_TIMER_TG2, TC_2_4_GetVersion) PASS
TEST(DRV_TIMER_TG2, TC_2_5_ControlNotOpen) PASS
TEST(DRV_TIMER_TG2, TC_2_6_infoGet) PASS
TEST(DRV_TIMER_TG3, TC_3_1_CloseSuccess) PASS
TEST(DRV_TIMER_TG3, TC_3_2_CloseHdl) PASS
TEST(DRV_TIMER_TG3, TC_3_3_CloseNotOpen) PASS

-----------------------

36 Tests 0 Failures 0 Ignored 36 Pass
```

Continuous Integration

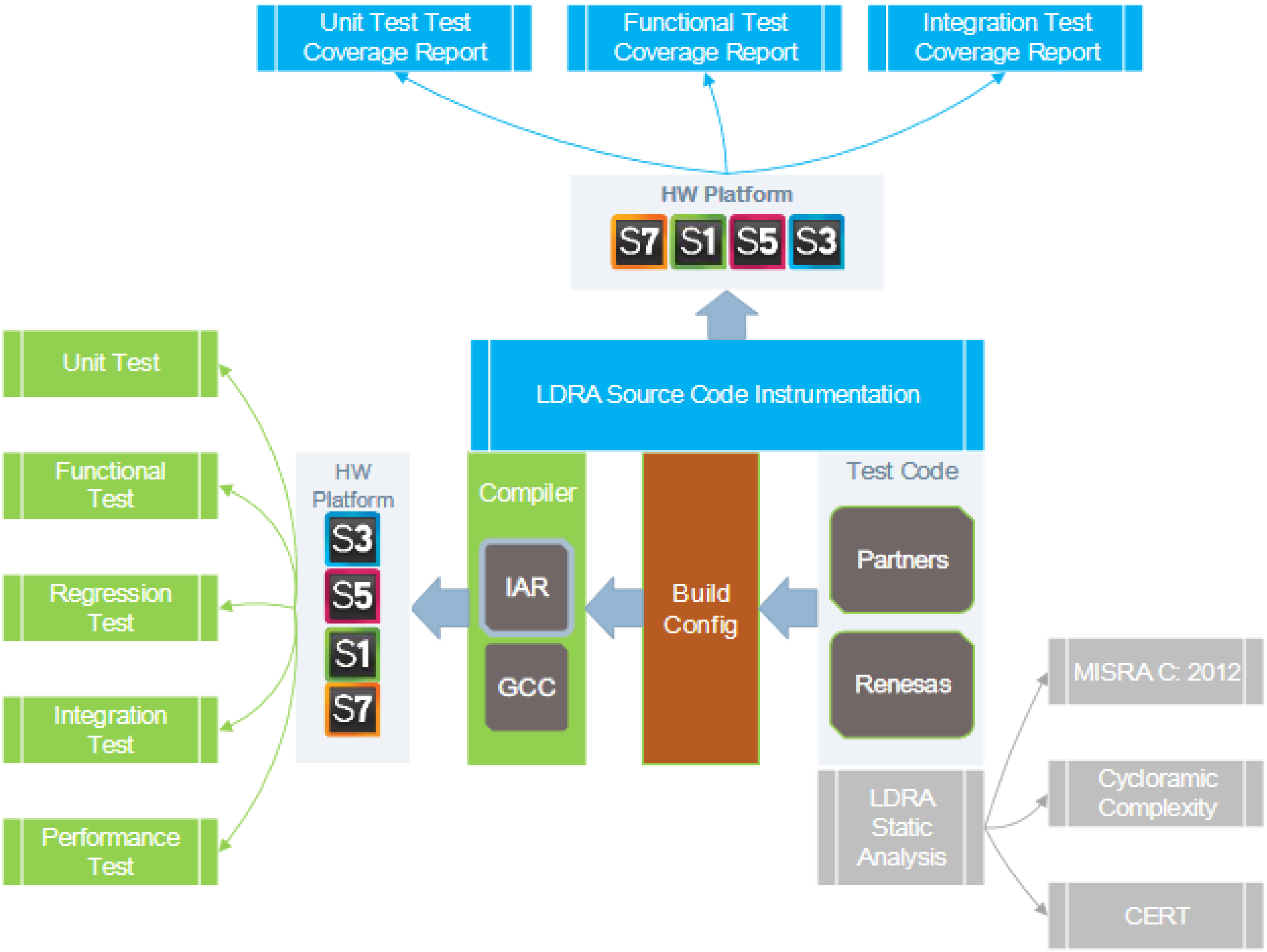


Image Source: Renesas Synergy Quality Manual

Automated Reporting

Synergy Software Package			Quality Matrices					Quality Data					Functional Test		Software Unit Tests												Verification Index Score			
Test ID	SSP Modules Name	Quality Index	Clean Build Index	Coverage Index	Complexity Index [1]	Coding Standard Index [2]	Verification Index	Test Coverage (statement/Decision)	Max Complexity	Coding Standard	warning	Backward Compatibility [3]	Automated Test Coverage (Statement / Decision)	Tests	Development Test Coverage (Statement / Decision)	s7g2	s5d9	s5d5	s5d3	s3a7	s3a6	s3a3	s3a1	s1ja	s128	s124	Tested on all HWs [4]	Tests Traceable	Tests Passed	Test Matrix Complete
1	bsp	100%	5	5	5	5	5	(100/100)	13	0	0	1	(88/80)	193	(4/38)	31	33	33	33	33	33	33	33	33	33	31	1	1	2	1
2	r_acmphs *	100%	5	5	5	5	5	(100/100)	10	0	0	1	(0/0)	33	(83/70)	9	9	9	10	9				9			1	1	2	1
3	r_acmplp *	100%	5	5	5	5	5	(100/100)	8	0	0	1	(0/0)	27	(84/71)		6			10	10	10	10	10	10	10	1	1	2	1
4	r_adc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	255	(93/89)	45	45	45	9	45	45	45	45	45	45	45	1	1	2	1
5	r_agt	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	116	(92/89)	33	33	33	45	33	33	33	33	33	33	33	1	1	2	1
6	r_agt_input_capture	100%	5	5	5	5	5	(100/100)	13	0	0	1	(85/79)	35	(100/100)	22	22	22	33	22	22	22	22		22	22	1	1	2	1
7	r_analog_connect	100%	5	5	5	5	5	(100/100)	7	0	0	1	(79/74)	40	(70/62)	3	3	3	22	5	4	4	4	5	5	4	1	1	2	1
8	r_cac	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	122	(98/94)	24	24	24	3	24	24	24	24	24	24	24	1	1	2	1
9	r_can	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	180	(100/100)	40	40	40	24	40	40	40	40	40	40	40	1	1	2	1
10	r_cgc	100%	5	5	5	5	5	(100/100)	15	0	0	1	(90/81)	294	(87/82)	94	94	94	40	94	94	94	94	70	70	70	1	1	2	1
11	r_crc	100%	5	5	5	5	5	(100/100)	8	0	0	1	(100/100)	80	(86/80)	10	10	10	94	10	10	10	10	10	10	10	1	1	2	1
12	r_ctsu	60%	5	5	0	0	5	(100/100)	84	247	0	1	(94/87)	229	(31/21)	14	14	14		14					13	13	1	1	2	1
13	r_dac	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	56	(100/100)	34	34	34	10	34	34	34	34	34		34	1	1	2	1
14	r_dac8	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	50	(95/94)		14					37	37	37	37		1	1	2	1
15	r_dmac	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	117	(96/92)	29	29	29	34	29	29	29	29				1	1	2	1
16	r_doc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	52	(99/96)	7	7	7	29	7	7	7	7	7	7	7	1	1	2	1
17	r_dtc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	111	(96/93)	28	28	28	7	28	28	28	28	28	28	28	1	1	2	1
18	r_elc	100%	5	5	5	5	5	(100/100)	5	0	0	1	(100/100)	48	(80/62)	7	7	7	28	7	7	7	7	7	7	7	1	1	2	1
19	r_flash_hp	100%	5	5	5	5	5	(100/100)	10	0	0	1	(96/95)	184	(93/86)	29	29	29	7								1	1	2	1

Image Source: Renesas

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Additional Resources

- Supporting Materials
  - Beningo.com
  - Blog
  - Code, White Papers, Courses
- Embedded Bytes Newsletter
  - http://bit.ly/1BAHYXm

From www.beningo.com under

- Blog > CEC – Designing and Launching an Embedded Product