Introduction to Software Defined Radio (SDR) - A Hands-on Course

Class 5: Commercial SDR Designs

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Presented by:

This Week's Agenda

9/25 Intro to SDR

9/26 RF and Radio Basics

9/27 Exploring SDR with the RTL-SDR, Part 1

9/28 Exploring SDR with the RTL-SDR, Part 2

9/29 Commercial SDR Designs

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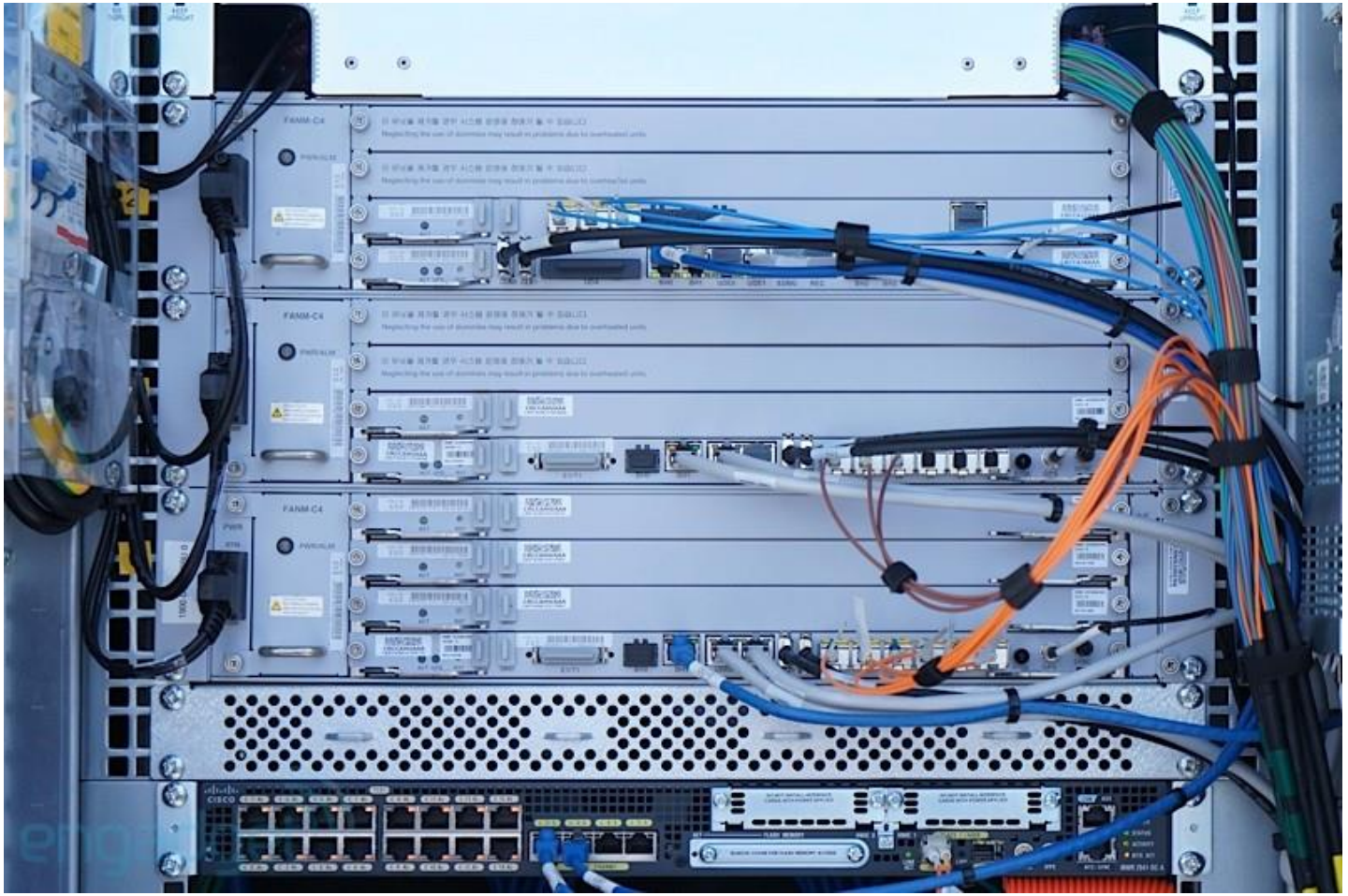
First in Cellular…

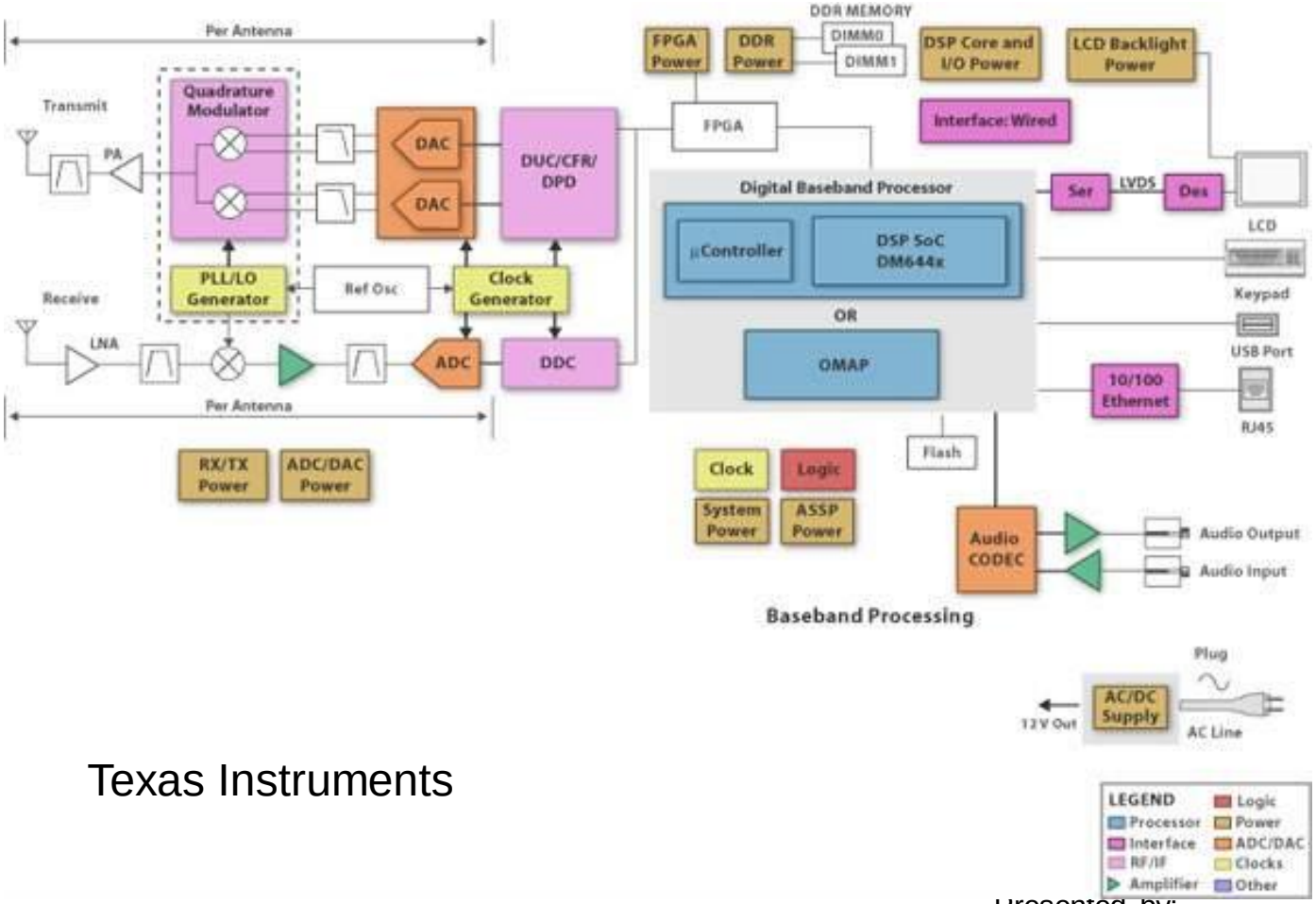


To the Battlefield…

SDRs come in many forms

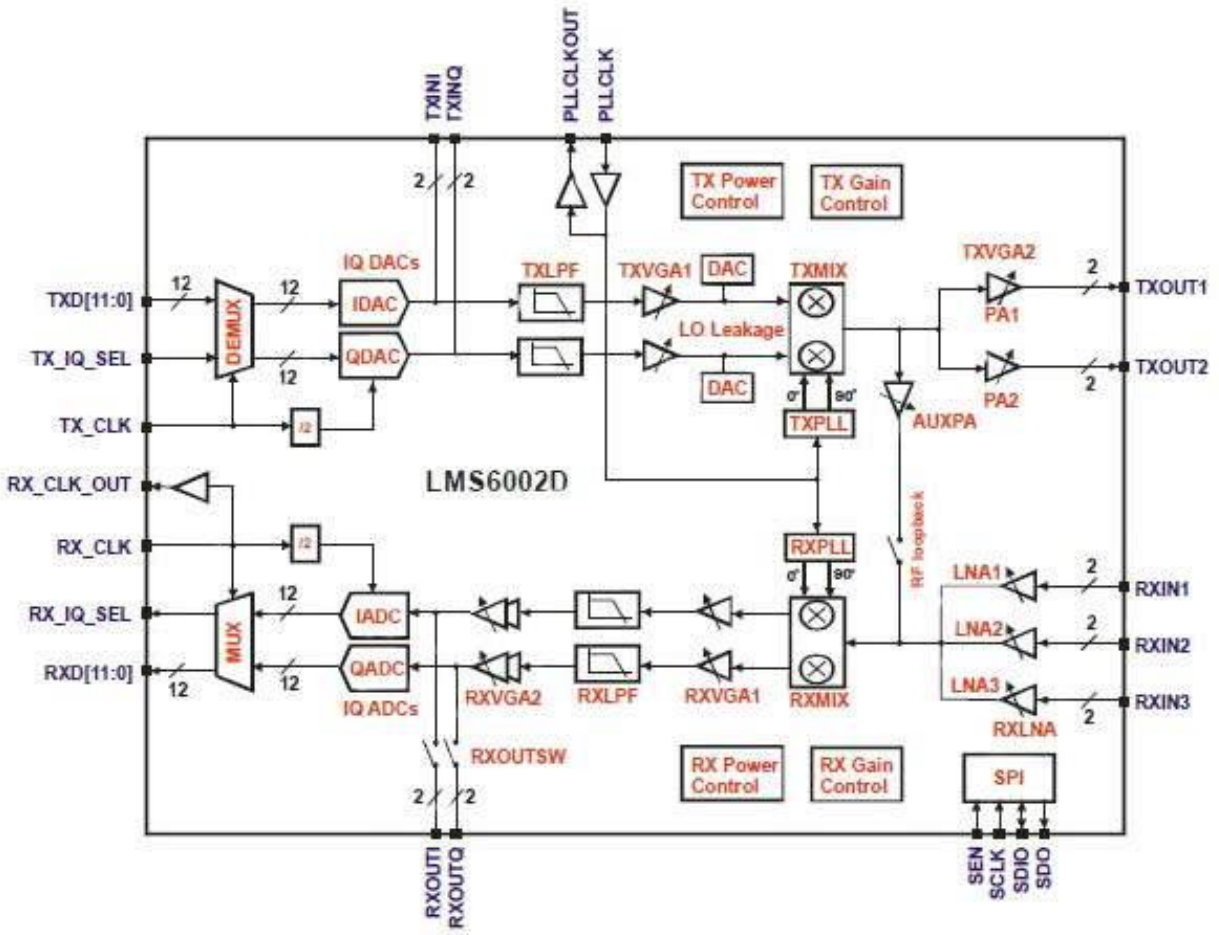
Question 1 - Can you identify the radio on the left?

Typical Block Diagram



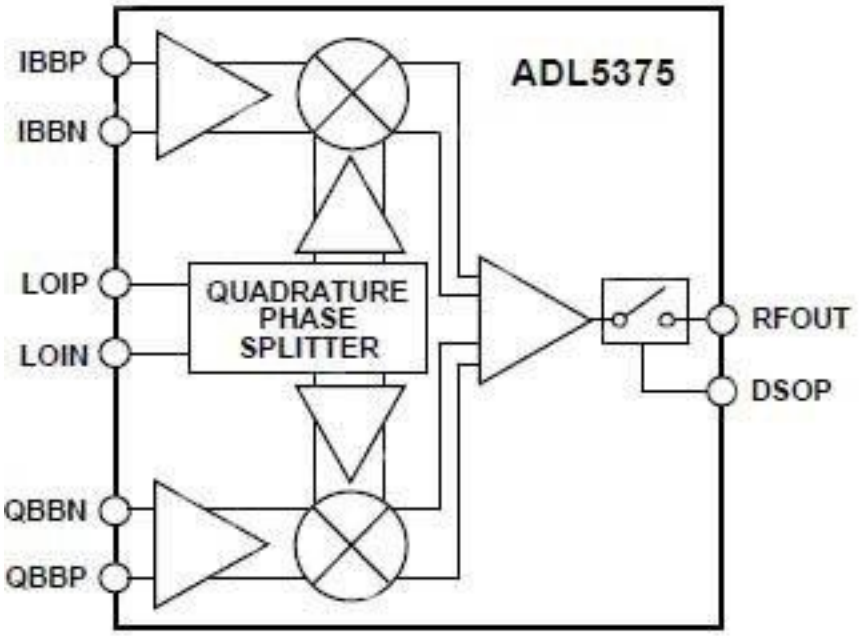
Texas Instruments

Lime Microsystems LMS6002D integrated front-end for SDR

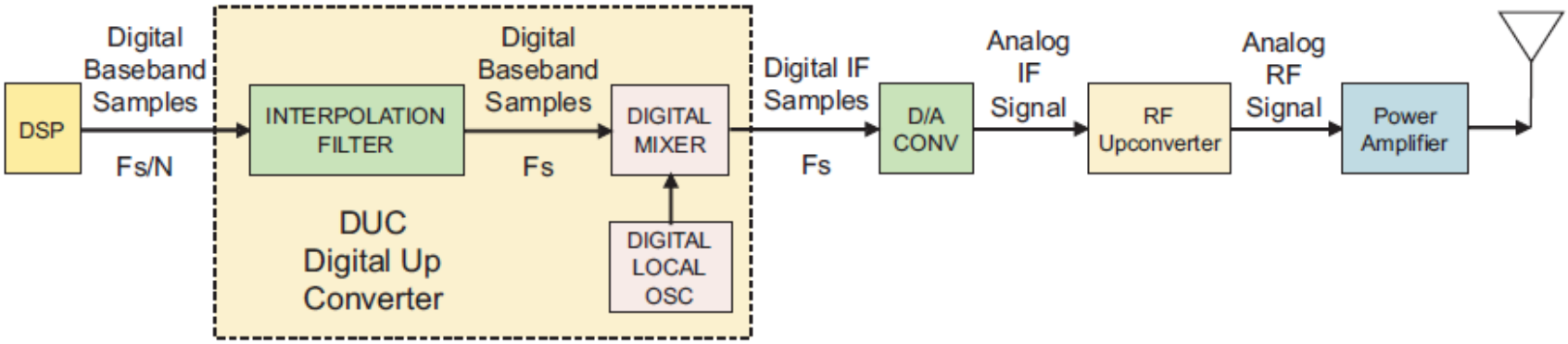


MYRIADRF Board from Lime

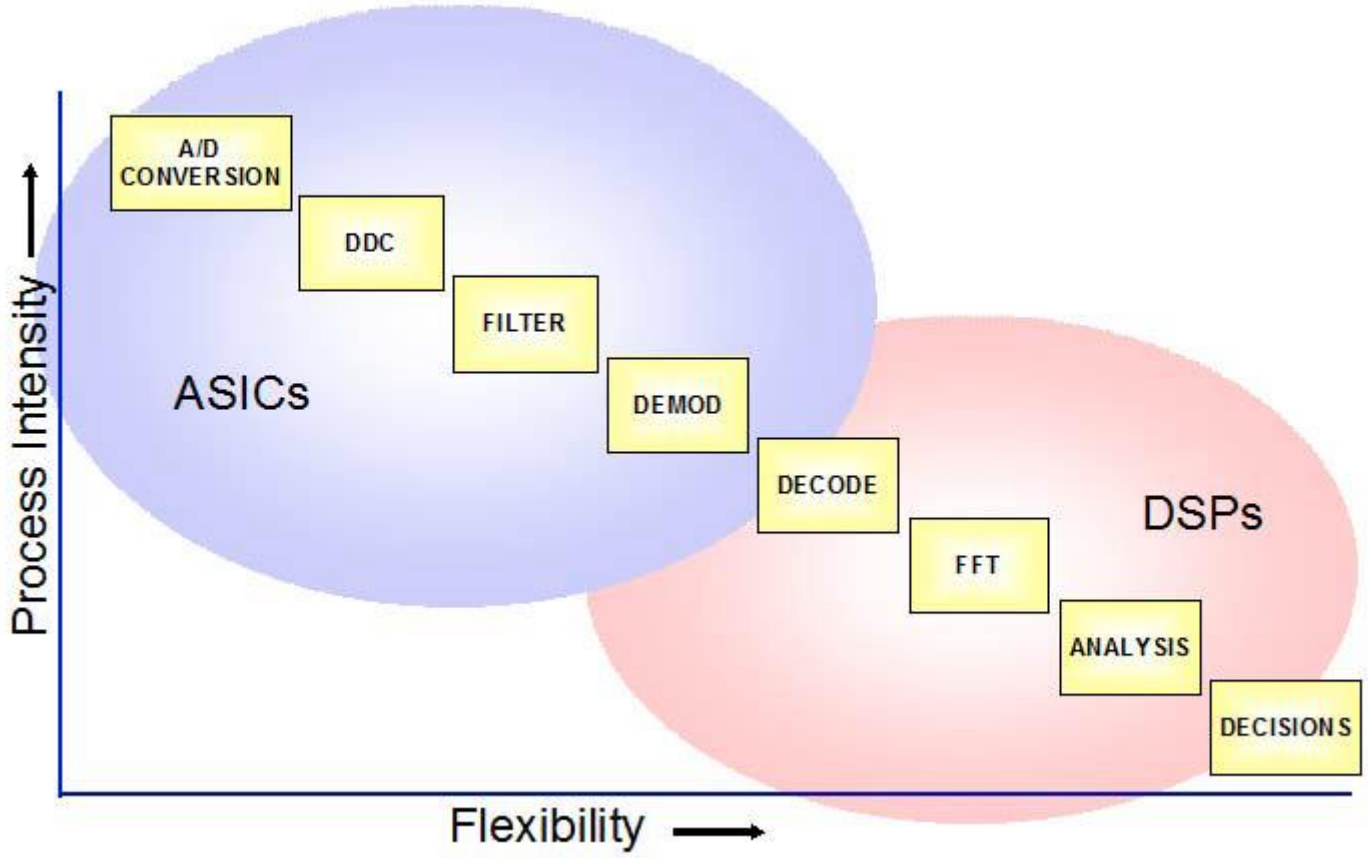
Analog Devices ADL 5375



Basic SDR Transmitter



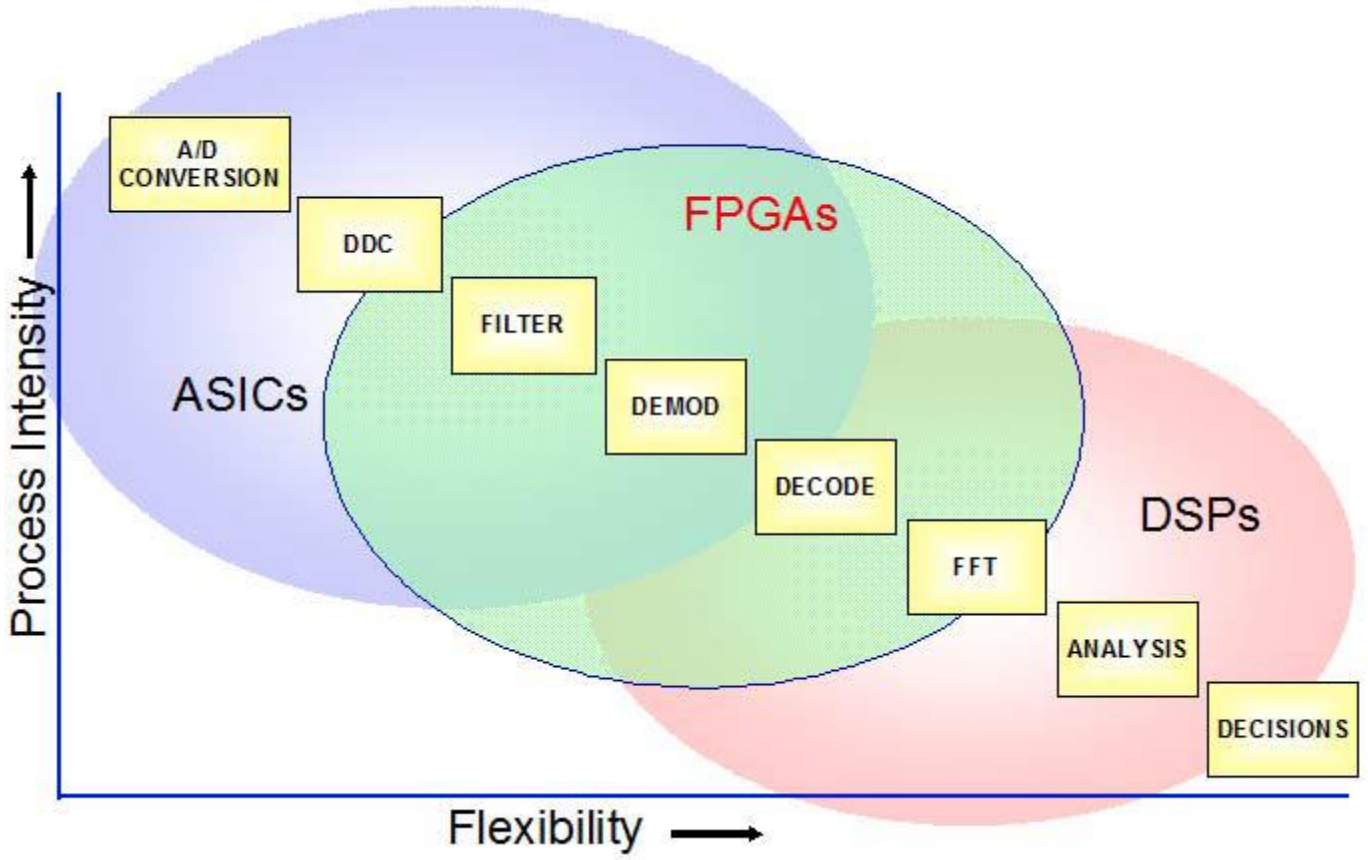
Block Diagram vs Technology



FPGAs in SDR

- Parallel Processing
- Hardware Multipliers for DSP
  - FPGAs can now have over 500 hardware multipliers
- Flexible Memory Structures
  - Dual port RAM, FIFOs, shift registers, look up tables, etc.
- Parallel and Pipelined Data Flow
  - Systolic simultaneous data movement
- Flexible I/O
  - Supports a variety of devices, buses and interface standards
- High Speed
- Available IP cores optimized for special functions

FPGAs are making work easier



Some High-End Xilinx FPGAs

	Virtex-5 LX, SX	Virtex-6 LX, SX	Virtex-7 VX	Kintex KU035, 60,115
Logic Cells	52K–155K	128K–314K	326K–693K	444K–1,451K
CLB Flip-Flops	32K–96K	160K–392K	408K–864K	406K –1,326K
Slices*	8K–24K	20K–49K	51K–108K	69K–207K
Block RAM (kb)	4,752–8,784	9,504–25,344	27,000–52,920	19,000–75,900
DSP Slices	128–640	480–1,344	1,120–3,600	1,700–5,520
Serial Gbit Transceivers	12–16	20–24	28–80	16–64
PCI Express Support	N/A	Gen 2 x8	Gen 2 x8, Gen3 x8	Gen 2 x8, Gen3 x8
Max. User I/O	480–680	600–720	700–1,000	416–676

*Virtex-5, Virtex-6, Virtex-7 and Kintex Slices actually represent 6.4 Logic Cells

Tradeoffs

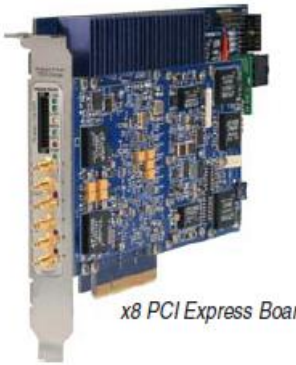
- High-end FPGAs can also mean higher-cost per device
- Power consumption and multiple power supplies
- Development tools may be limited
- Design for Test is critical!

Question 2 – What are some other considerations of using FPGAs?

Examples of Pentek SDR Modules

XMC Module

3U VPX Boards
COTS and Rugged



x8 PCI Express Board

AMC Board

6U CompactPCI
Board

PMC/XMC
Module

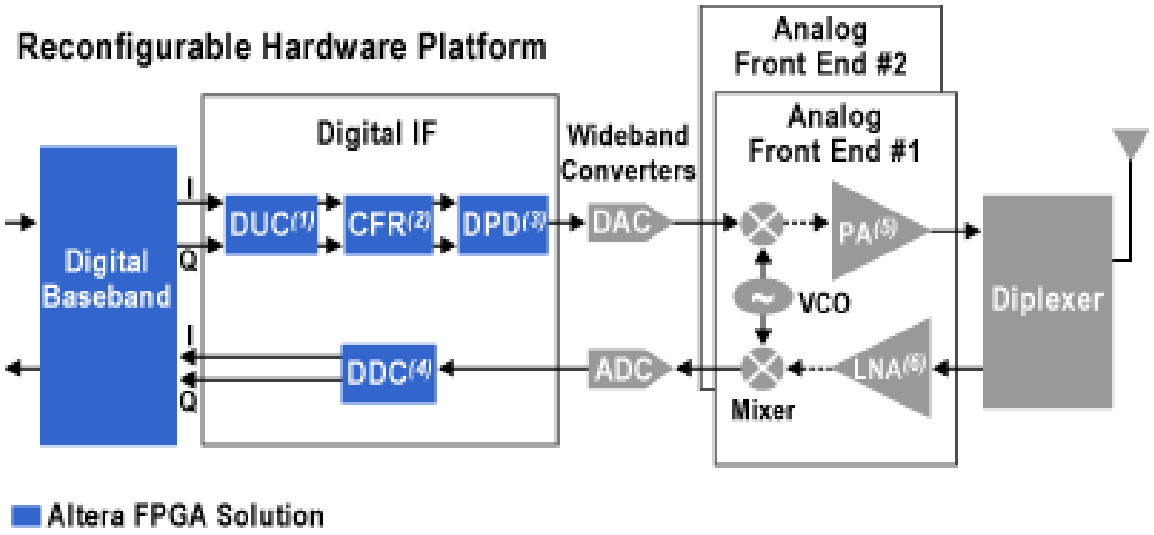
FMC Carrier

FMC I/O Module

6U VPX
Board

Architectures of SDR

1. *SDR Architecture Based on Current-Generation Technology*



Notes to Figure 1:

- DUC: Digital upconverter DDC: Digital downconverter
- CFR: Crest factor reduction DPD: Digital predistortion
- PA: Power amplifier LNA: Low noise amplifier

2. Software Architecture of SDR

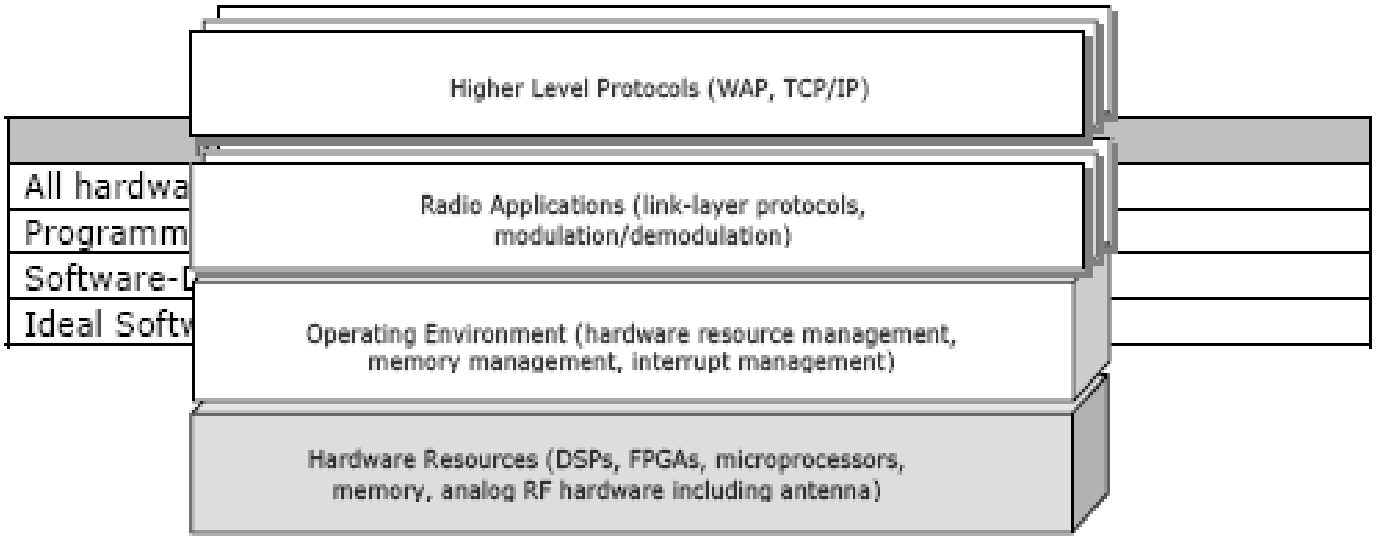
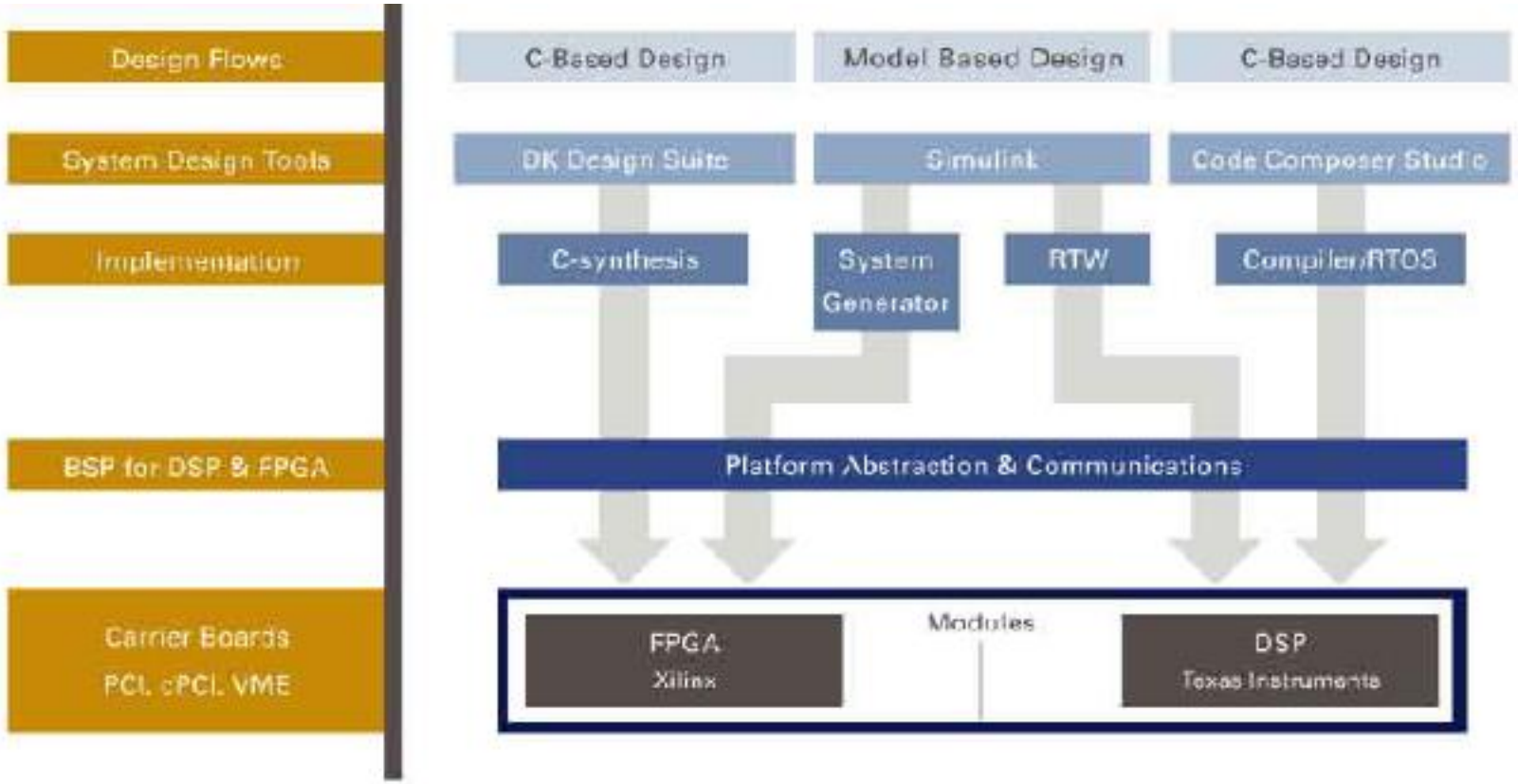


Figure 2: Software Architecture of SDR

1) The system uses a generic hardware platform with programmable modules (DSPs, FPGAs, microprocessors) and analog RF modules. The operating environment performs hardware resource management activities like allocation of hardware resources to different applications, memory management, interrupt servicing and providing a consistent interface to hardware modules for use by applications.

2) In SDR system, the software modules that implement link-layer protocols and modulation/demodulation operations are called radio applications and these applications provide link-layer services to higher layer communication protocols such as WAP and TCP/IP.

Computer Architecture

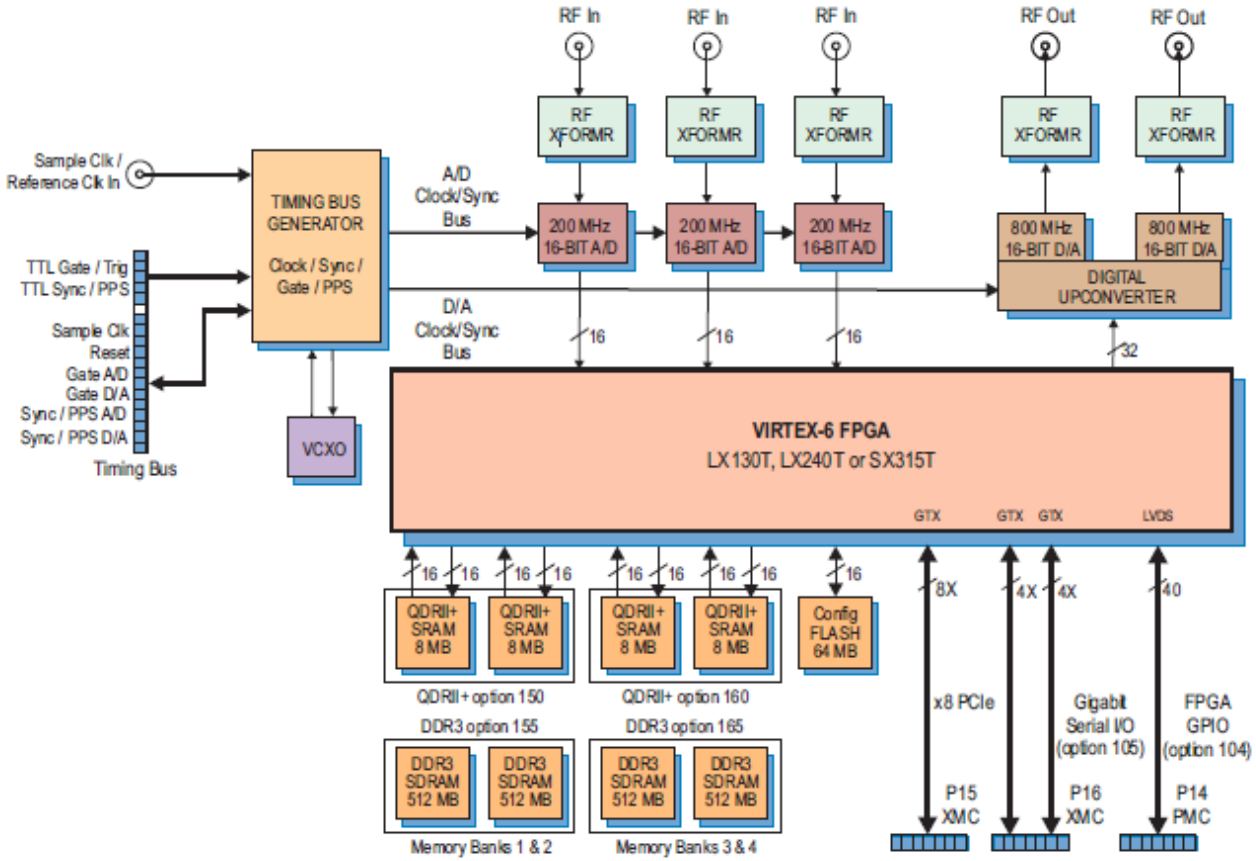


Typical Components of SDR

- Analog Radio Frequency (RF) receiver/transmitter in the 200 MHz to multi-gigahertz range.
- High-speed A/D and D/A converters to digitize a wide portion of the spectrum at 25 to 210 Msamples/sec.
- High-speed front-end signal processing including Digital Down Conversion (DDC) consisting of one or more chains of mix + filter + decimate or up conversion.
- Protocol-specific processing such as Wideband Code Division Multiple Access (W-CDMA) or OFDM, including spreading/de-spreading, frequency-hop-and chip-rate recovery, code/decode functions, including modulation/demodulation, carrier and symbol rate recovery, and channel interleaving/de-interleaving.
- Data communications interface with carrier networks and backbone for data I/O and command-and-control processing, usually handled by general purpose ARM or PowerPC processors and Real-Time Operating System (RTOS).

Pentek Cobalt

Model 71620
XMC



HackRF One

- 1 MHz to 6 GHz operating frequency
- Half-duplex transceiver
- Up to 20 million samples per second
- 8-bit quadrature samples (8-bit I and 8-bit Q)
- Compatible with GNU Radio, SDR#, and more
- Open source hardware
- Software-configurable RX and TX gain and baseband filter
- Software-controlled antenna port power (50 mA at 3.3 V)
- SMA female antenna connector
- SMA female clock input and output for synchronization
- Convenient buttons for programming
- Internal pin headers for expansion
- Hi-Speed USB 2.0 - USB-powered

$300

Question 3 – Would you be interested in a class on this unit?

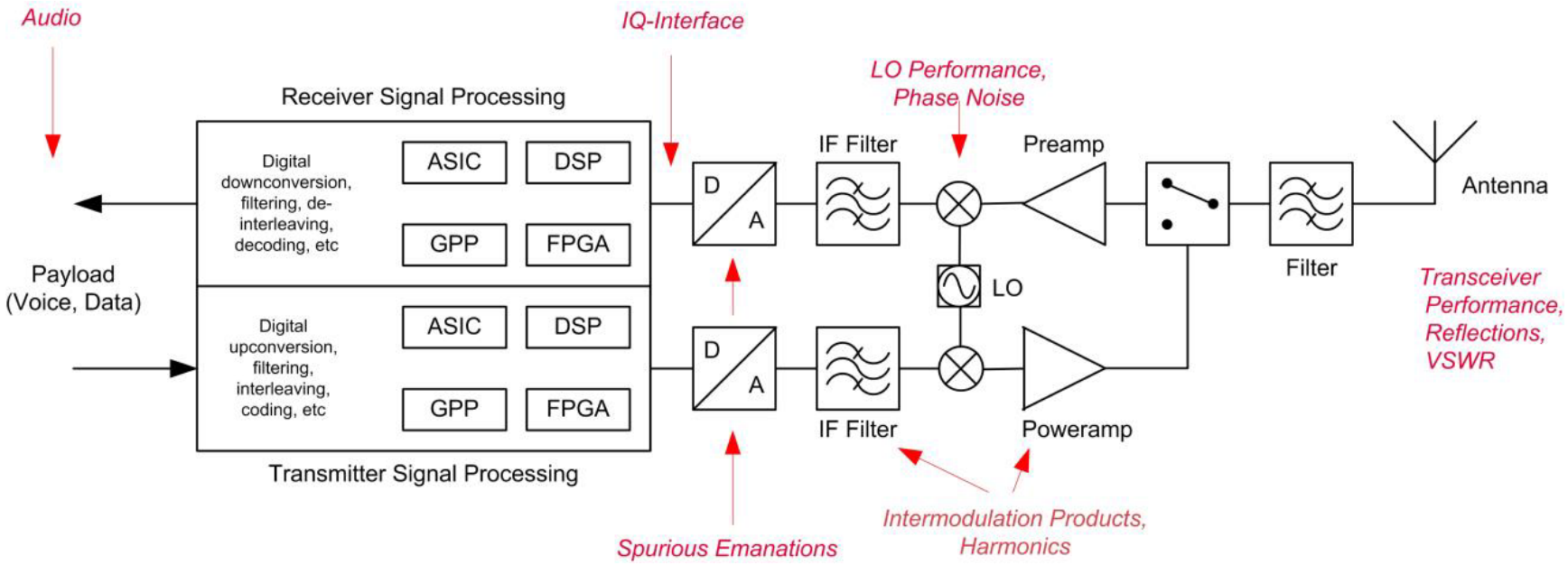
SDR Platforms

- Wind River VxWorks 6.2 Commercial Grade Real-Time Platform
- Xilinx Virtex-II Platform FPGA
- Texas Instruments TMS320C6713 DSP
- Sundance's SMT8096 platform
  - The SMT8096 is a rapid-prototyping solution package, comprised of an SMT310Q PCI Carrier hosting SMT395 DSP and SMT350 ADC/DAC modules.
- Altera's Stratix Professional Edition
  - It includes a Stratix II DSP development board, the DSP Builder design tool, Quartus II development software, MATLAB/Simulink evaluation software, evaluation intellectual property (IP) cores
- Pentek

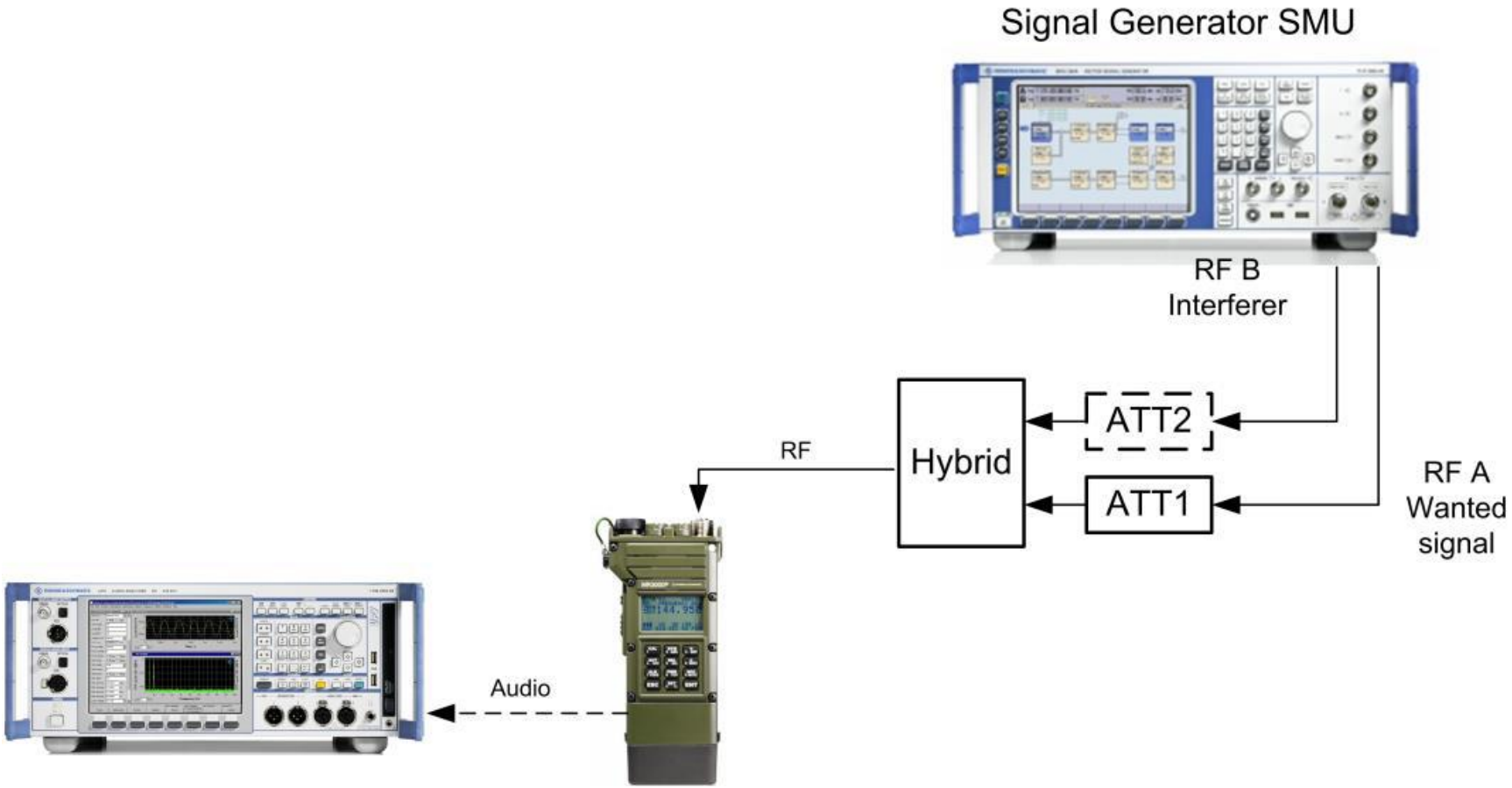
Development Tools

- Zeligsoft CE (Component Enabler)
- Green Hill's INTEGRITY RTOS & PJFS
- Mathwork's Simulink & Matlab
- Celoxica's DK Design Suite
- Xilinx Virtex-II Pro family and XtremeDSP initiative
- Code Composer Studio™ Development Tools and 3L Diamond applications
- Spectrum Signal Processing's SDR-3000 Solutions
- Pentek Navigator

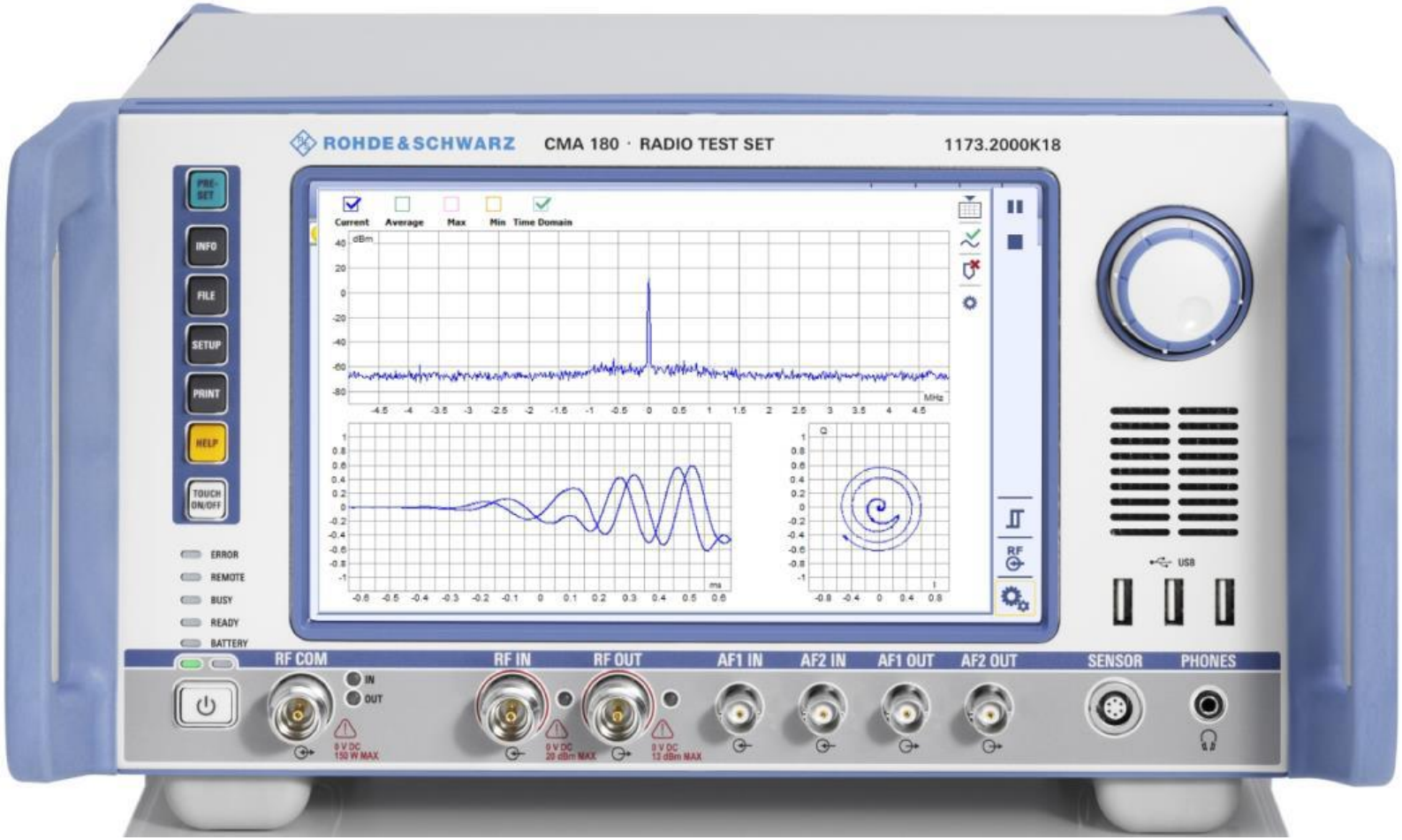
Testing of SDRs



Selectivity (Same as for Analog)



Communications Monitor



Conclusions

- SDR development is still growing
- FPGA and ASICs will continue to dominate
- Prices for lower-end will continue to drop
- Analog filters are still important!
- Much to be developed in antennas still

$$\Delta\theta(n) = \frac{i(n)\frac{d[q(n)]}{dn} - q(n)\frac{d[i(n)]}{dn}}{i^2(n) + q^2(n)}$$

Can be fun!

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Question 4

- What classes would YOU like to see?
- I have a class on LoRaWAN coming up here in December
- Working on possibles:
  - Circuit Studio Hands On
  - Circuit Maker Hands On
  - Implementing PKI in your IoT (Hands On)
  - 6LowPAN Hands On
  - Developing IoT Security Standards
  - Talk to the IoT – Novel HMI Ideas

Please stick around as I answer your questions!

- Please give me a moment to scroll back through the chat window to find your questions
- I will stay on chat as long as it takes to answer!
- I am available to answer simple questions or to consult (or offer in-house training for your company)
  c.j.lord@ieee.org
  http://www.blueridgetechnc.com
  http://www.linkedin.com/in/charleslord
  Twitter: @charleslord
  https://www.github.com/bradatraining