



# Implementing Embedded Vision: Designing Systems That See and Understand Their Environments

## When to Use FPGAs to Accelerate Embedded Vision Applications

March 21<sup>th</sup>, 2013

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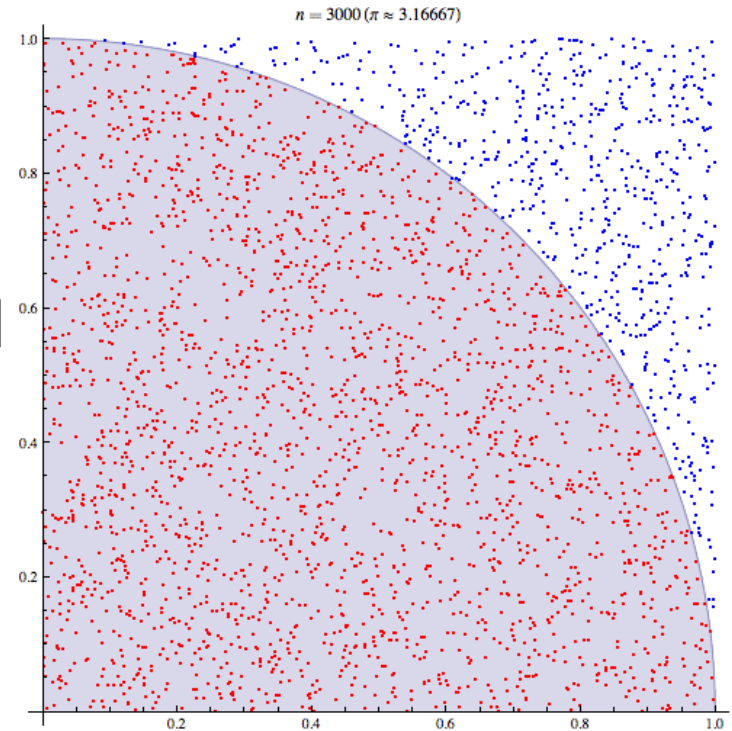


# When to Use FPGAs to Accelerate Embedded Vision Applications

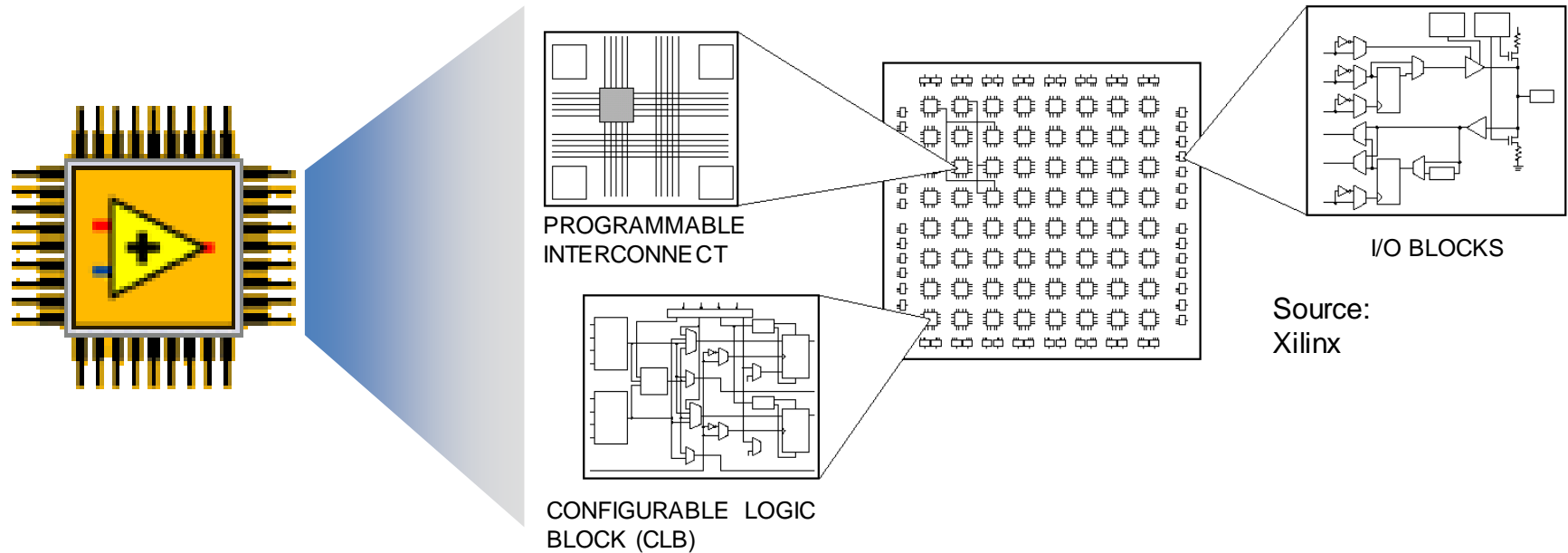
- Who am I?
- Who are you?
- What we will talk about today

# Accelerating CPU systems

- Ride the CPU frequency wave
- Automatic hardware acceleration (SSE, Hyperthreading)
- Making software multithreaded
  - OpenMP (multiple cores)
  - MPI (multiple separate machines)
  - Many others
- Some problems divide well
- Others don't



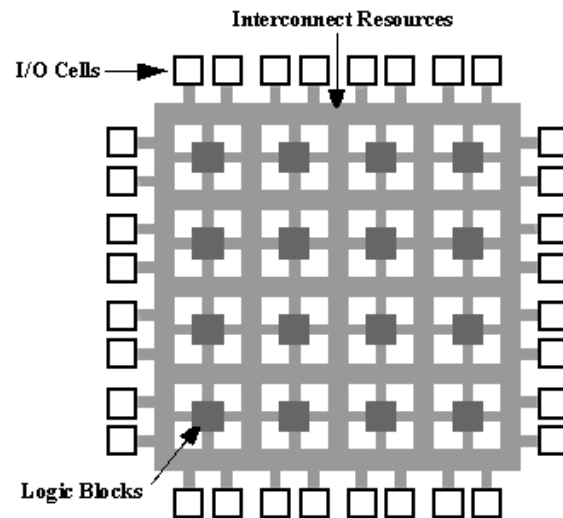
# Field Programmable Gate Array (FPGA)



A semi-conductor device containing many gates (logic devices). A wiring list downloaded to the FPGA determines the gate connections and the functionality.

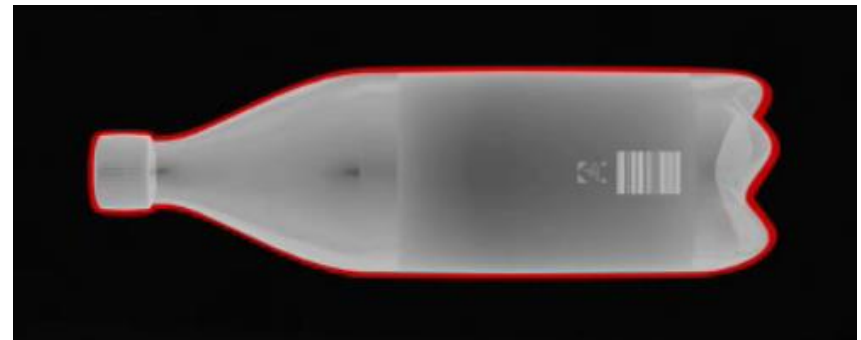
# Software-Defined Hardware = FPGA

- Software Programmable (and Reconfigurable)
- Hardware Reliable (and Repeatable)
- High-speed Signal Processing (and Parallel Processing)
- Extreme Determinism (and clock-cycle control)



## An Example “Pfandautomat”

- Germany’s Bottle Recycling System
- System Checks the following
  - UPC code
  - Size, of the Bottle
- Prints Voucher or Returns Bottle



## Example Continued

- Can an FPGA do all the tasks?
  - Yes, but....




FPGA

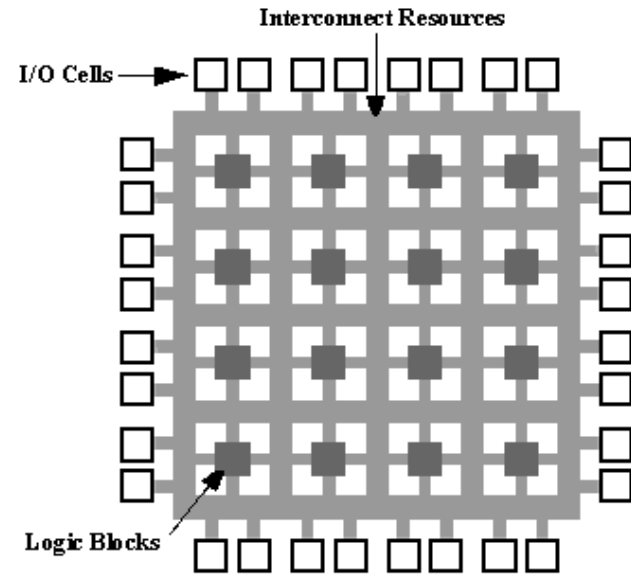
- Reads through every line of the image
- Adjust lens / contrast / focus for image quality
- Search for the UPC code image
- Captures complete UPC code image

Processor

- Decode the UPC number
- Search database
- Match database to characteristics
- Issue refund or return bottle to user

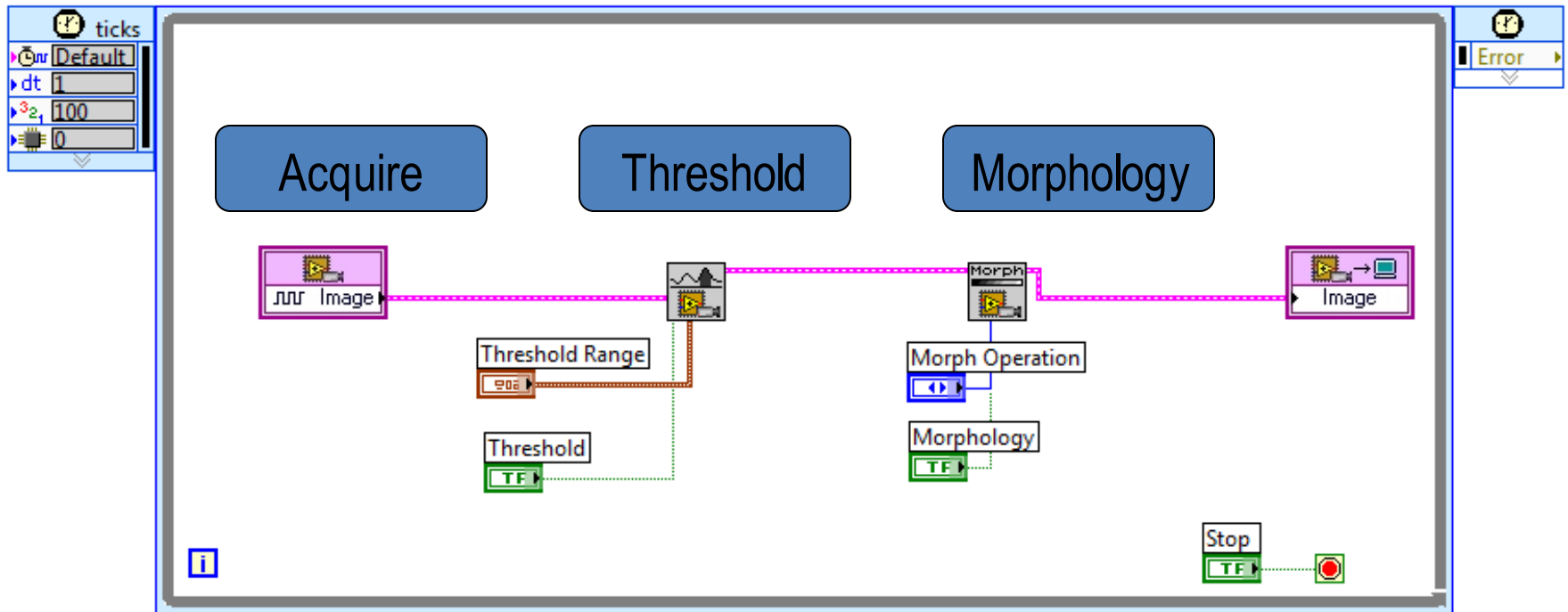
# FPGAs

- Latency 
- Jitter 
- Compute power 
- Pipelining
- Security
- Weight / Power / Heat
- Complexity
- Raw Clock Rates
- Limited Floating Point support



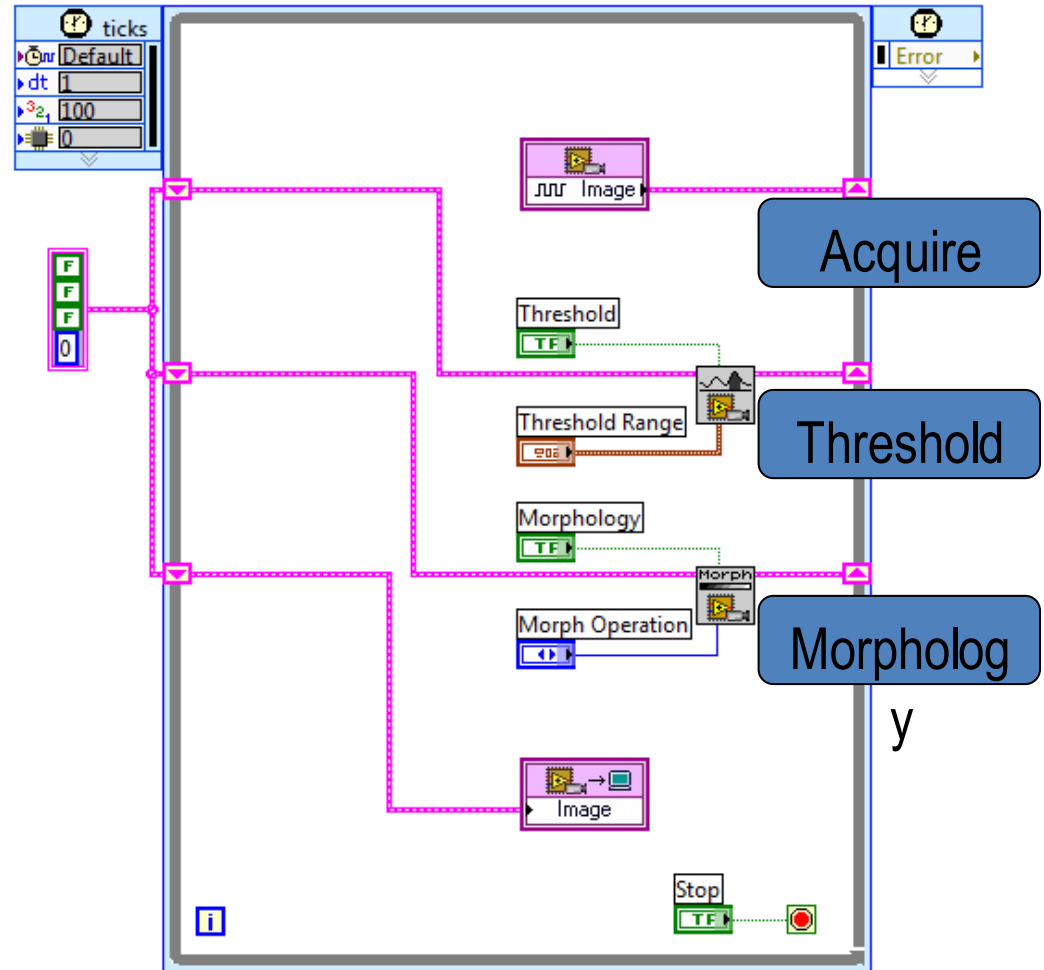


# Sequential Image Processing



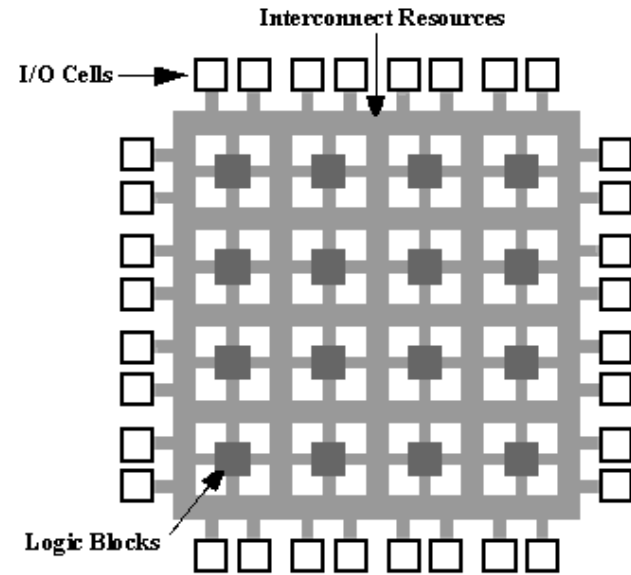
# Pipelining

- Processing loop rate limited by longest delay in loop
- Reduce delays by splitting operations into multiple cycles
- Increases speed, but also latency



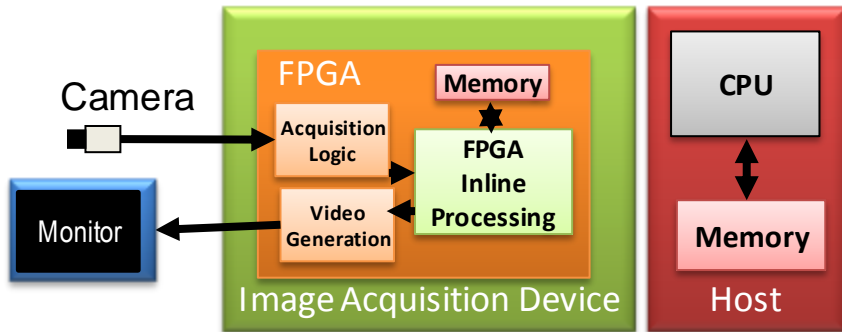
# FPGAs

- Latency ✓
- Jitter ✓
- Compute power ✓
- Pipelining ✓
- Security ✓
- Weight / Power / Heat ✓
- Complexity
- Raw Clock Rates
- Limited Floating Point support

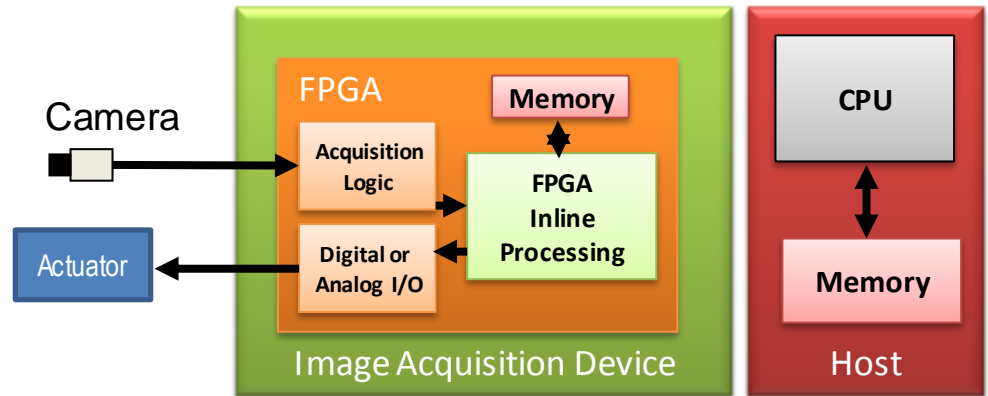


# FPGA Use Modes

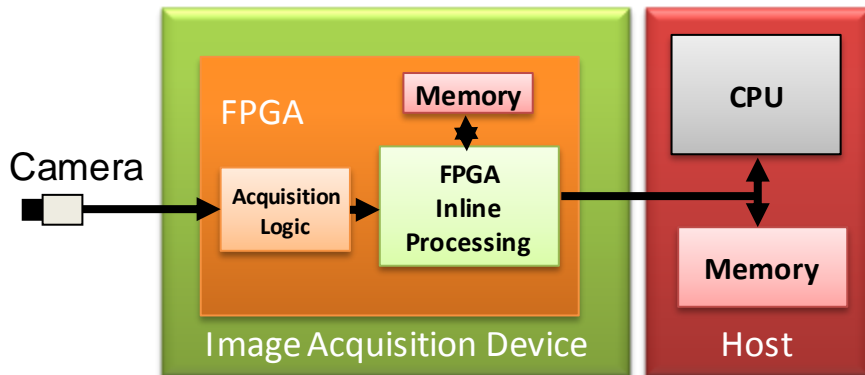
**Visualization**



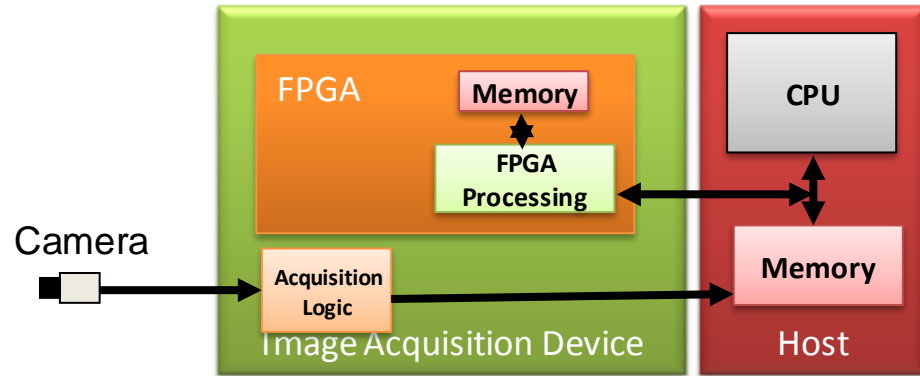
**High-speed Control**



**Image Preprocessing**

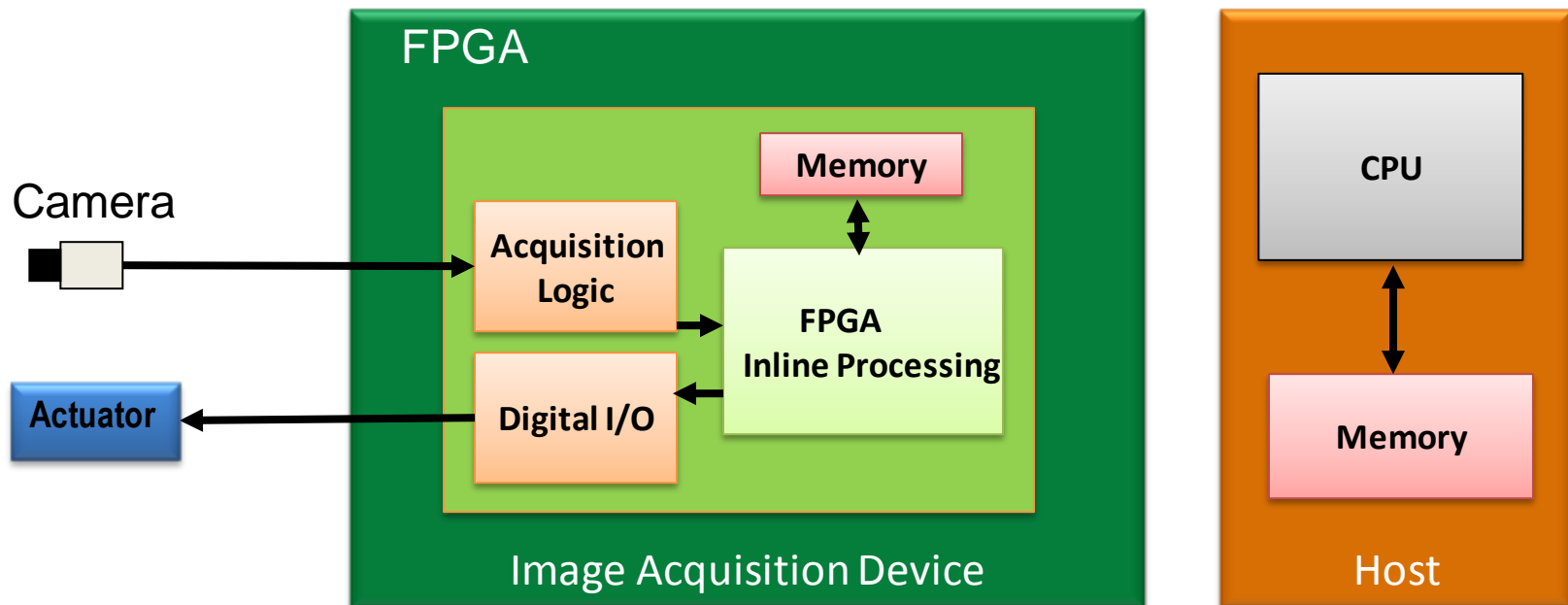


**Co-Processing**



# High-Speed Control

- FPGA is directly in the path of the image data
- FPGA generates and outputs control commands directly

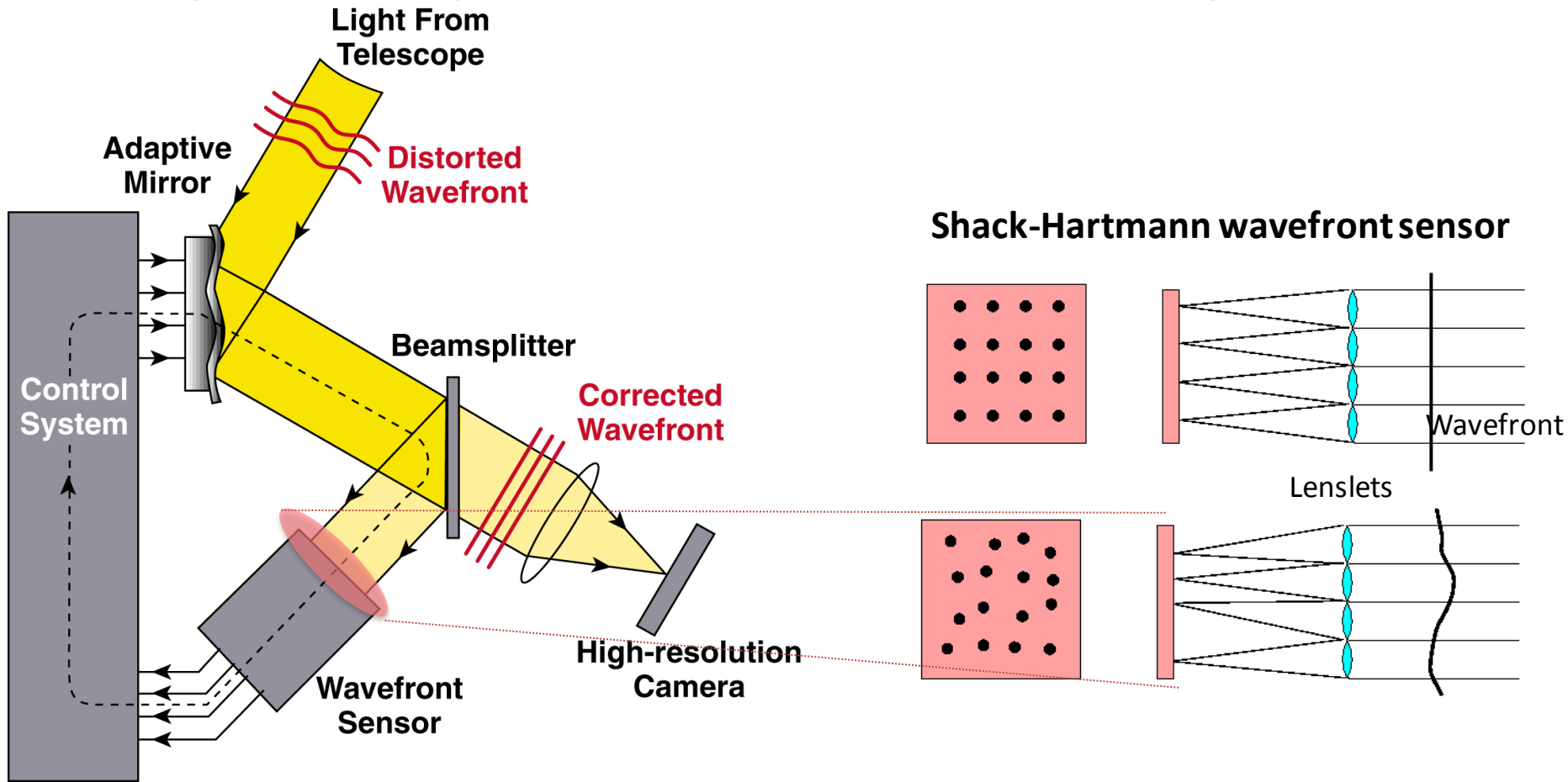


# High-Speed Control

- Laser alignment/steering
  - Beam profile/position measurements
  - Low latency control output
- High-speed sorting
  - Segmentation
  - Measure parameters of contaminant
  - Trigger rejection valves
- In Air Sorting
  - Image and inspect falling product
  - Low jitter requirement for decision making and IO

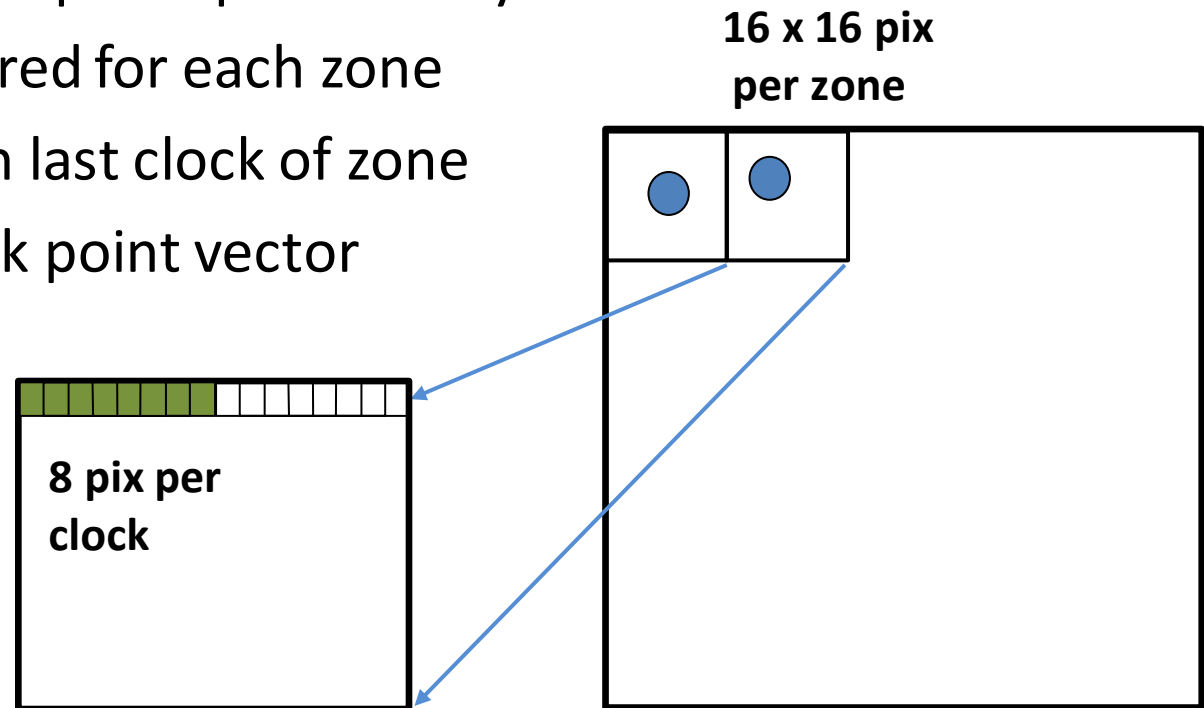


# Adaptive Optics – Centroid Computation



# Adaptive Optics – Centroid Computation

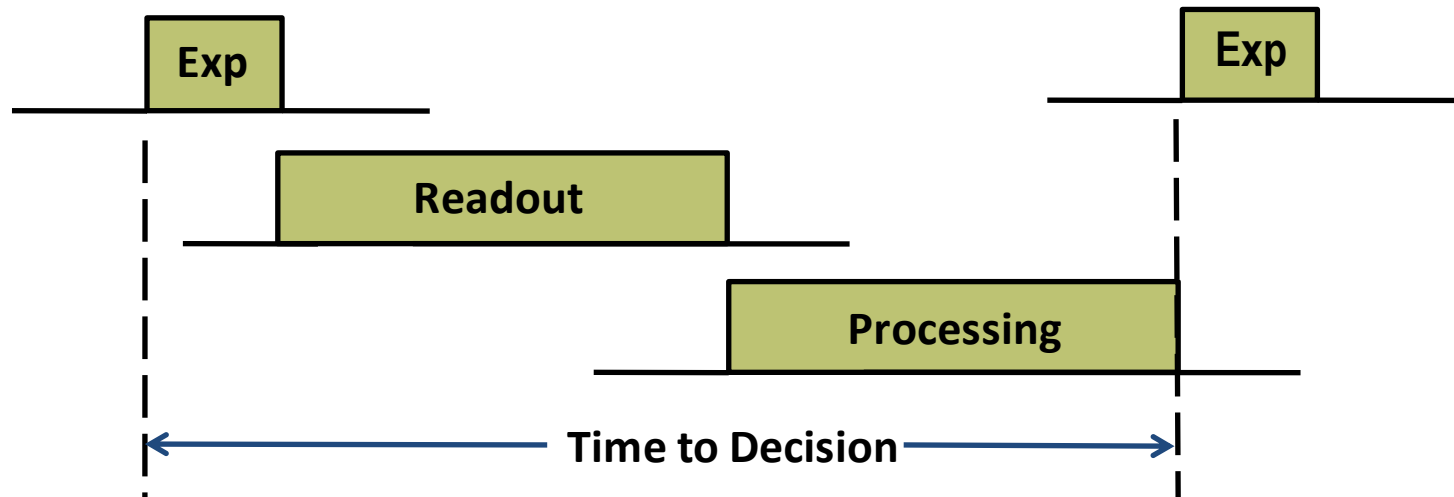
- 512 x 512 image divided into 16 x 16 pixel zones (1024 total)
- Camera transmits 8 pixels per clock cycle
- Running sums stored for each zone
- Centroid divide on last clock of zone
- Data reduced to 1k point vector





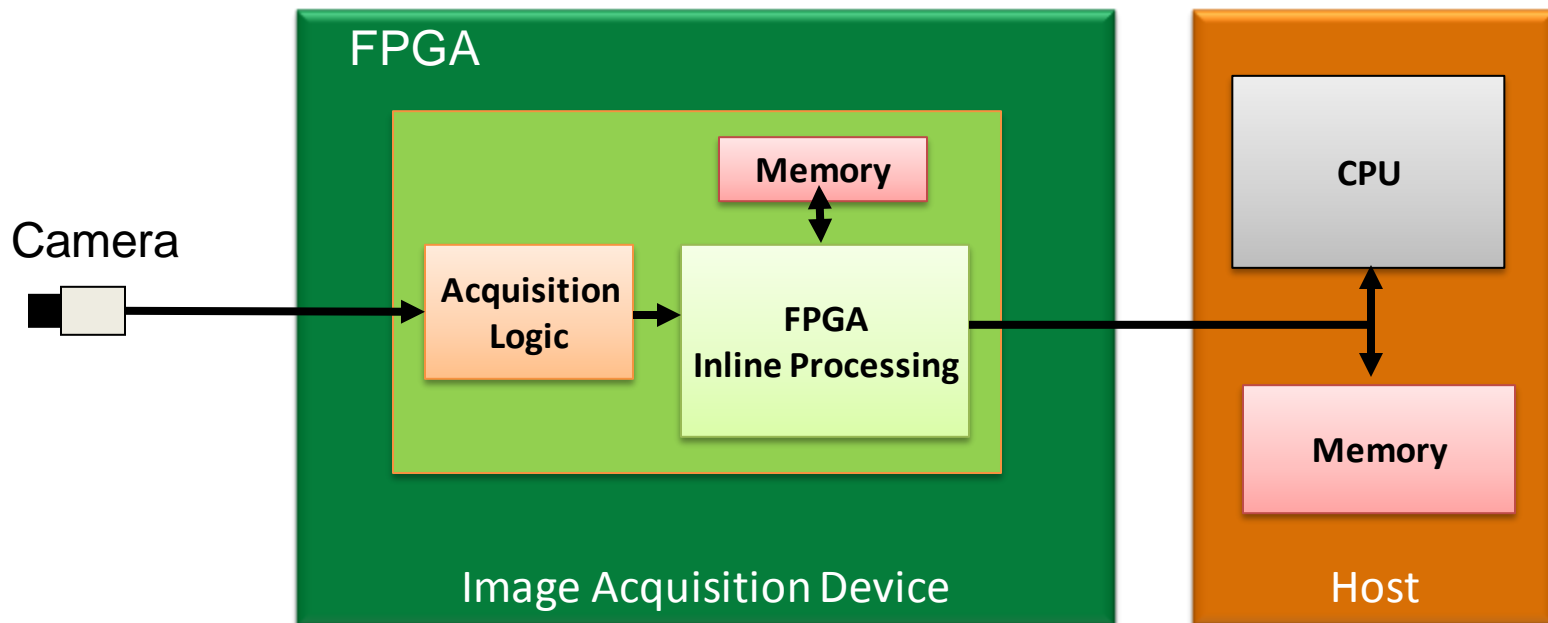
# Adaptive Optics – Centroid Computation

- Host based vision starts processing after image transmitted
- FPGA vision can start on first pixel and finish shortly after last pixel
- Latency reduced by almost 1 frame period
- Start of exposure to last result available  $\sim 600\mu\text{s}$



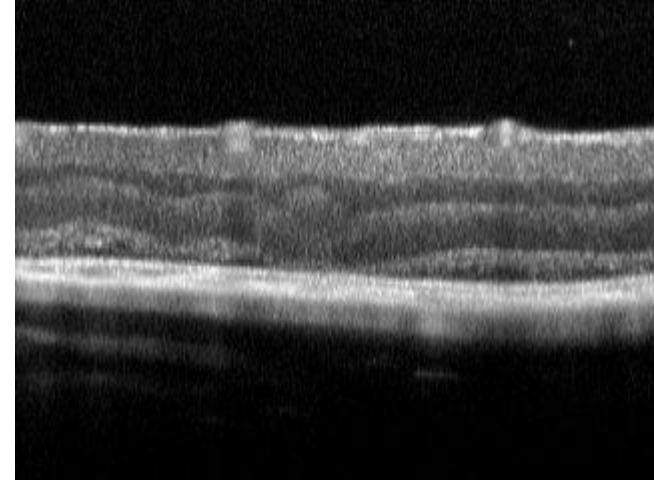
# Image Pre-processing

- FPGA is directly in the path of the image data
- Processes pixels as they arrive
- Final image processing handled by the host CPU



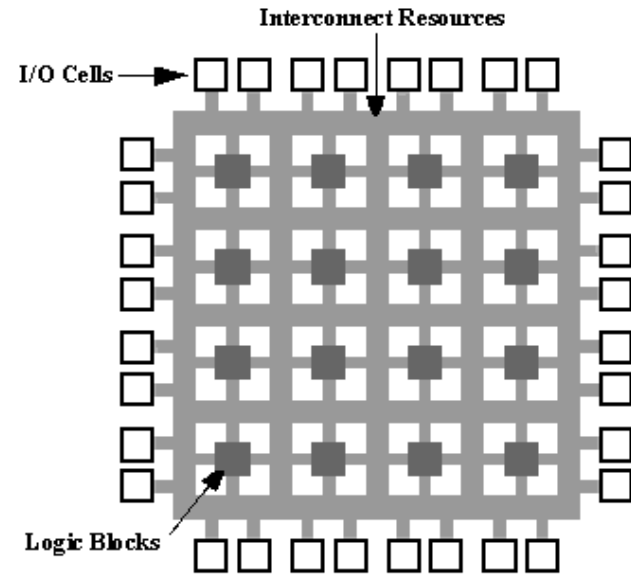
# Image Pre-processing

- Optical Coherence Tomography (OCT)
  - Data scaling
  - FFT
  - Logarithmic LUT
  - Image display (host)
  
- Web and surface inspection
  - Flat field correction
  - Thresholding
  - Particle analysis



# FPGAs

- Latency ✓
- Jitter ✓
- Compute power ✓
- Pipelining ✓
- Security ✓
- Weight / Power / Heat ✓
- Complexity **X**
- Raw Clock Rates **X**
- Limited Floating Point support **X**



## Starting an FPGA Vision Project

- Create an FPGA value statement
  - What is the value an FPGA is adding?
- Model the algorithm in software
  - Have you chosen the right algorithm?
- Compare FPGA behavior with a bit-accurate software model
  - Have you implemented the FPGA version of the algorithm correctly?

## The Embedded Vision Alliance

### *Free Resources on Embedded Computer Vision*

The Embedded Vision Alliance web site, at [www.Embedded-Vision.com](http://www.Embedded-Vision.com), covers embedded vision applications and technology, including interviews and demonstrations



Register on the Alliance web site for free access to:

- The Embedded Vision Academy—free in-depth tutorial articles, video “chalk talks,” code examples, and discussion forums.
- Embedded Vision Insights—bimonthly newsletter with industry news and updates on new resources available on the Alliance website.



Embedded Vision Insights

*The Latest Developments on Designing Machines that See*

Embedded vision technology and services companies interested in becoming sponsoring members of the Alliance may contact [info@Embedded-Vision.com](mailto:info@Embedded-Vision.com)

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## *Embedded Vision Summit*

**A Free Educational Event for Engineers—San Jose, April 25<sup>th</sup>**

Learn how to use the hottest new technology in the industry to create “machines that see”

- Technical presentations on sensors, processors, tools, and design techniques
- Keynote by Prof. Pieter Abbeel, UC Berkeley, a leader in developing machine intelligence
- Cool demonstrations and opportunities to meet with leading vision technology suppliers

Co-located with UBM Electronics’ DESIGN West

- DESIGN West also includes the Embedded Systems Conference, Black Hat Summit, and exhibits

The Summit is free, but space is limited. To register to attend, go to [www.embedded-vision.com/embedded-vision-summit](http://www.embedded-vision.com/embedded-vision-summit)

