





Interfacing to and Processing Data from Image Sensors

March 19th 2013 Jose Roberto Alvarez Engineering Director Xilinx, Inc







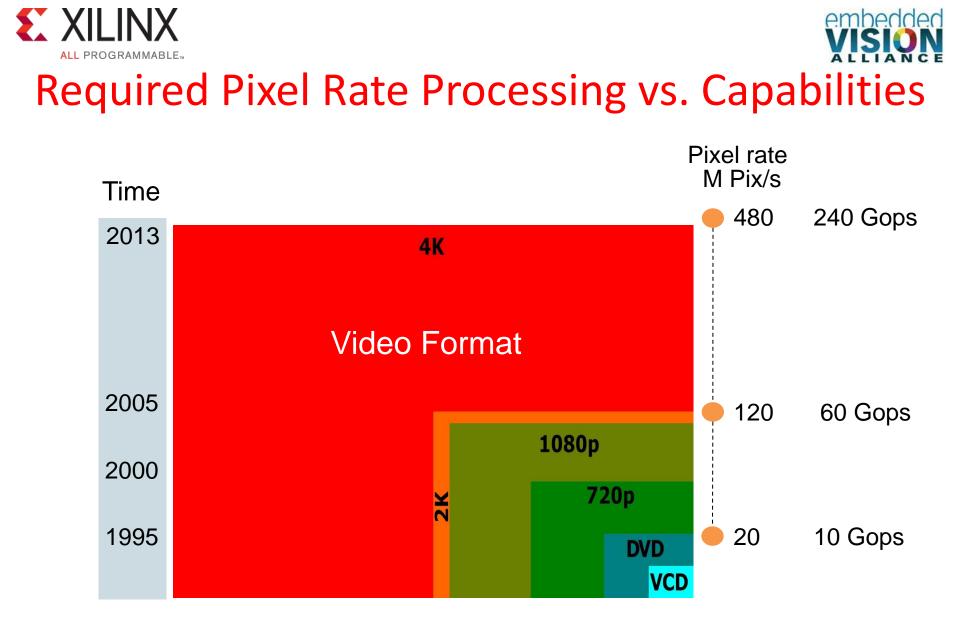


Image Sensor considerations

- Image size
 - CIF, SD, HD, etc.
- Frame rates
 - 30 Fps, 60 Fps, 120 Fps
- Data width
 - Bits per word (8,10, 12, ...)
 - Endianess
 - Word Ordering (RBG, BGR, GBR, ...)
- Data Formats
 - Parallel, serial, rgb, bgr, gbr
- Color Spaces
 - RGB, CMY, etc.
- Synchronization
 - Blanking, active video, hsync, vsync













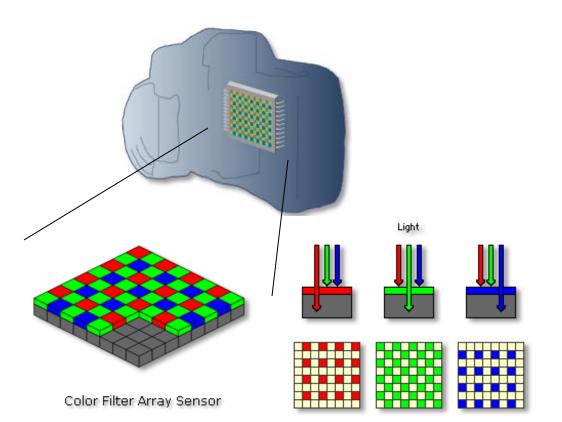
Data Rates – 8 Mpix sensor

Hsize	Vsize	Bits	Pic/sec	BW
3840	2160	8	30	1.99 Gbps
			60	3.98 Gbps
3840	2160	12	30	2.99 Gbps
			60	5.97 Gbps
3840	2160	16	30	3.98 Gbps
			60	7.96 Gbps
Hsize	Vsize	Bit/pel	Pic/sec	BW
Hsize 3840	Vsize 2160	Bit/pel 24	Pic/sec 30	BW 5.97 Gbps
			30	5.97 Gbps
3840	2160	24	30 60	5.97 Gbps 11.9 Gbps
3840	2160	24	30 60 30	5.97 Gbps 11.9 Gbps 7.96 Gbps









- Dr. Bryce E. Bayer
- RGB, CMY







Imaging Sensor Subsampling

Twice as many Green elements



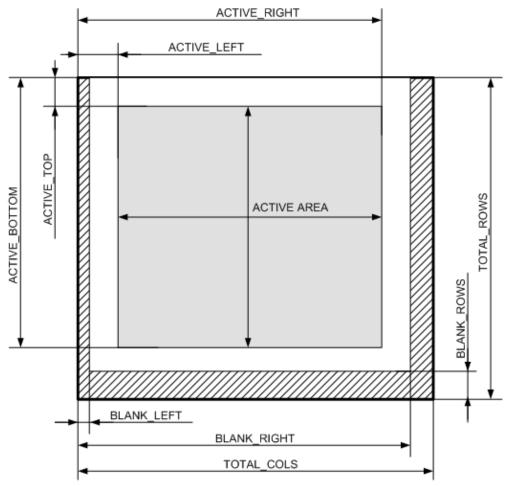




Timing Parameters

7

- ACTIVE_LEFT
- ACTIVE_RIGHT
- ACTIVE_TOP
- ACTIVE_BOTTOM
- TOTAL_ROWS
- TOTAL_COLS
- BLANK_ROWS
- BLANK_LEFT
- BLANK_RIGHT
- VBLANK_POLARITY
- HBLANK_POLARITY











Timing Signal Diagram

• timing signals: vblank, hblank, active_video

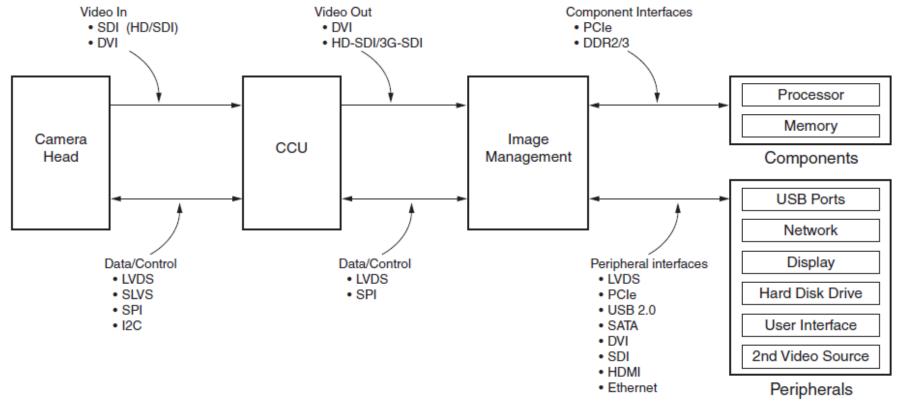
	000000000		ափափուփոփոփո	ս ուսիս փոփի	φαιφατιφί <u>φ</u> ιώται	<u>ការចុំកាត់កាត់ស្តាំថ្</u>	ឃុំឃុំឃុំហេប៉ុណប៉ុណ)փիս ուսփուփո	ចំពេរប៉ូពាចុំពារប៉ូ()		
vblank_in	0										
vblank_in hblank_in	0						1				
active_video_in	0	ſ									
video_data_out	234881039							<u>)</u>	ບໍ່ມາມີພໍ ນີ້ມີບໍ່ມານບໍ່ມ	φαιφαιφαιφήφαιφαιφαιφα	uuų́uu
vblank_out	1										
hblank_out	1										
active_video_out	1										







Common Interfaces in Camera Applications



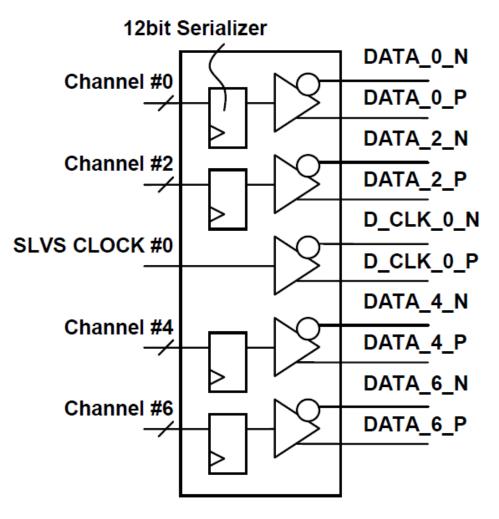
WP391_06_030411







Select I/O Resources



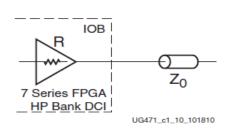
10

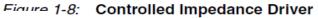


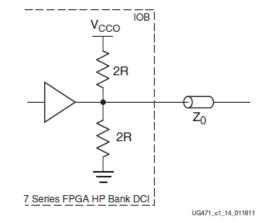




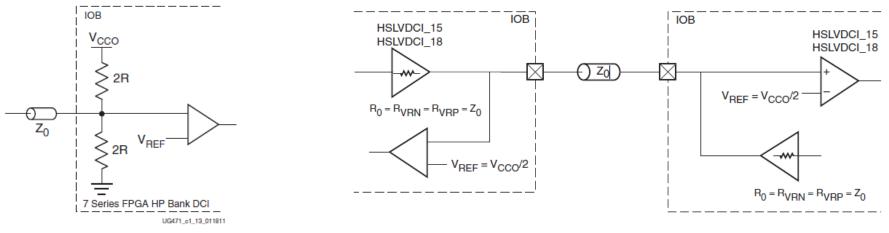
Select I/O Resources







Driver with Termination to $V_{CCO}/2$ Using DCI Split Termination



Input Termination to V_{CCO}/2 Using Split-Termination DCI

HSLVDCI Controlled Impedance Driver with Bidirectional Termination

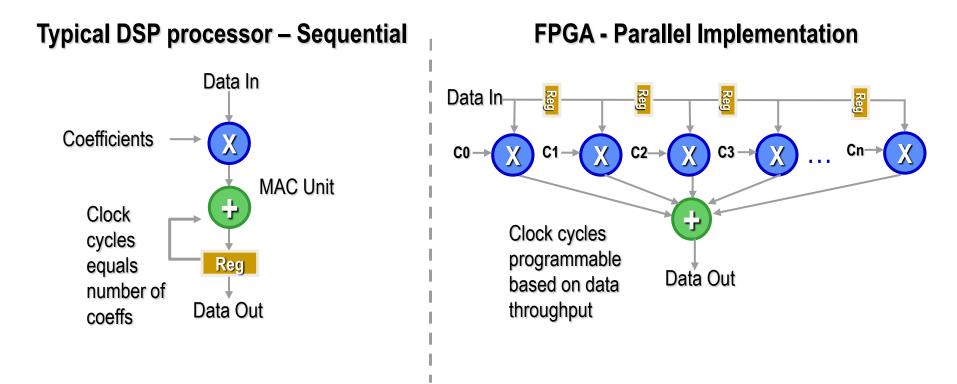








Image Data Processing







Typical Camera Processing Application

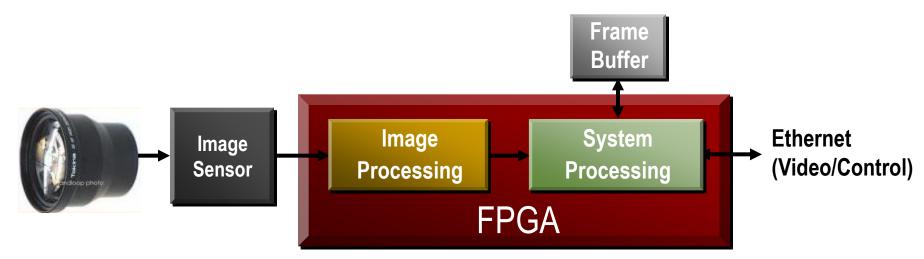


Image Processing

Base System

Defective Pixel Correction Color Filter Array Demosaic Color Correction Matrix Gamma Correction Color Space Conversion

Video Processing

Video Scaler On-Screen-Display Image Characterization

Extended System

Dark Noise Reduction Noise Reduction Chroma Resampler Picture Enhancement Statistics/3A example

System Processor MicroBlaze ™ 32-bit Soft Processor Dual Core ARM® Processors Linux/Software

Memory

Multi-port Memory Controller Video Frame Buffer Controller Hardened Memory Controller

Interfaces Tri-mode Ethernet MAC USB 2.0 UART GPIO GigE Vision, Camera Link Compression H.264

H.264 MPEG-2 Others

CONTINUING CENTER

System Processing



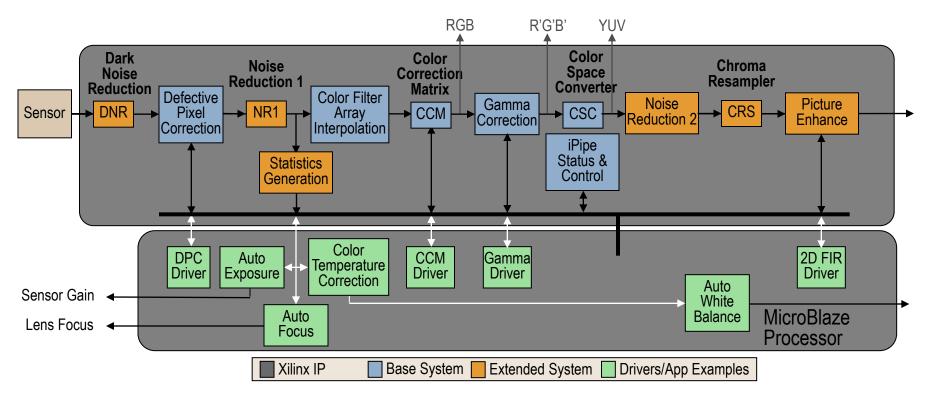
13







Xilinx Image Processing Pipeline



- Available as individual IP cores
- Reference Designs available







Defective Pixel Correction

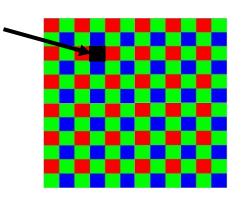
Single Pixel

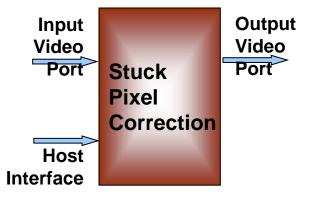
Corrects defective pixels that are:

- Static (always present)
- Defect Dynamic (function of temperature or exposure) Including:
 - Dead (always low)
 - Hot (always high)
 - Stuck (to a certain value)

Features

- Dynamic "On-the-fly" detection and correction
 - Each pixel is compared to the median value of
 - Nearest neighbors
 - Nearest neighbors in the same color plane
 - Programmable thresholds for each comparison
 - Pixels greater than one or more threshold are replaced with median value of nearest neighbors in the same color plane











G1	R2	G3	R4	G5
ļ	G7 <	1	G9	B10
G11	R12	G13	R14	G15
B16	G17		G19	B20
G21	R22	G23	R24	G25

B7 = (B6+B8) / 2



Ideal









G1	R	G3	R4	G5
B6	G7		G9	B10
G11	RI 2	G13	R14	G15
	G17		G19	B20
G21	R22	G23	R24	G25

R7 = (R2 + R12) / 2



Ideal









G1	R2	G.	R4	G5
B6	G7		0	B10
G11	R12	G <mark>1</mark> 3	R14	G15
	G1 7		G19	B20
G21	R22	G23	R24	G25

G8 = (G3+G7+G9+G13) / 4



Ideal









G1	P?	G3	R	G5
	G7	B8	G9	B10
G11	RI	G13	114	G15
	G17		G19	B20
G21	R22	G23	R24	G25

R8 = (R2 + R4 + R12 + R14) / 4



Ideal









G1	R2	G3	R4	G5
	G 7	B	G9	B10
G11	R12	G13	R14	G15
B' a	G1 7	V18	G19	B20
G21	R22	G23	R24	G25

B12 = (B6+B8+B16+B18) / 4



Ideal









G1	R2	G3	R4	G5
B6	G 7		G9	
G11	R12	G13	R14	G15
B16	G17		G19	
G21	R22	G23	R24	G25

- G8 = (G3+G7+G9+G13) / 4
- B7 = (B6+B8) / 2
- R7 = (R2+R12) / 2
- R8 = (R2+R4+R12+R14)/4
- B12 = (B6+B8+B16+B18) / 4



Ideal





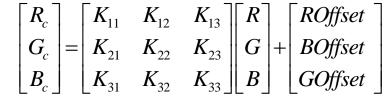




Color Correction Matrix



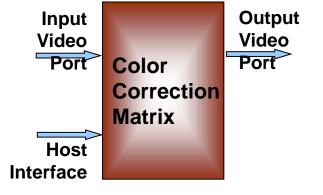
Uncorrected





Corrected

- Enables white balance, color cast, brightness and contrast corrections for RGB images
 - 3x3 programmable coefficient matrix multiplier with offset compensation
- Features:
 - Optimal resource usage and high performance
 - Optional CMY input to RGB output color conversion
 - Independent clipping and clamping control



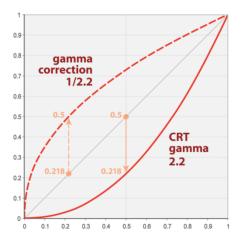






Gamma Correction

- Gamma correction (gamma compression, gamma encoding) encodes linear luminance or RGB values into video signals.
- Gamma expansion is the inverse, occurs in CRT monitors due the nonlinearity of the electron-gun current–voltage curve.
- Gamma correction is defined by $V_{out} = V_{in}^{\gamma}$, where the input and output values are between 0 and 1.
- The case γ <1 is gamma compression, γ >1 is gamma expansion.



23









Gamma Correction

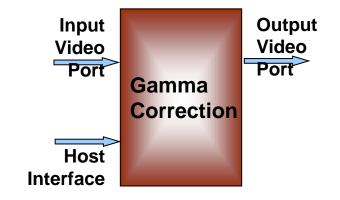
- Manipulates image data to match the response of display devices
 - Programmable Look-Up Table (LUT) Structure
- Features
 - Three implementation options:
 - Single LUT applied to all color channels
 - Independent LUT's for each of three colors
 - Multiple Block RAM usage optimization options
 - Multiple processor interface options







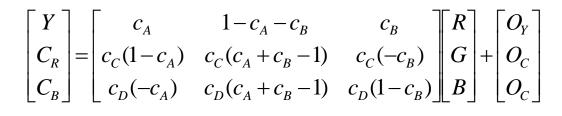


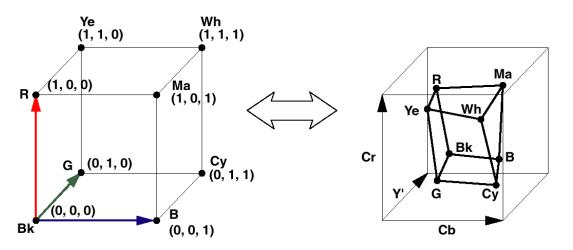






Color-Space Conversion









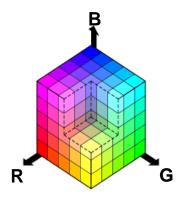


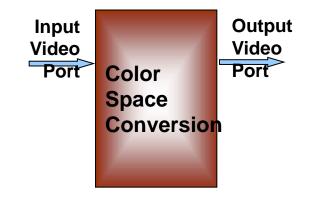
Color Space Converter

- RGB to YCrCb Color Space Converter
- YCrCb to RGB Color Space Converter
 - Simplified 3x3 matrix multiplier
 - Converts three input color samples to three output samples in a single CLK cycle

Features

- Built-in support for
 - SD (ITU 601)
 - HD (ITU 709) PAL
 - HD (ITU 709) NTSC
 - YUV
- User defined conversion matrices supported
- Optimal resource usage and high performance





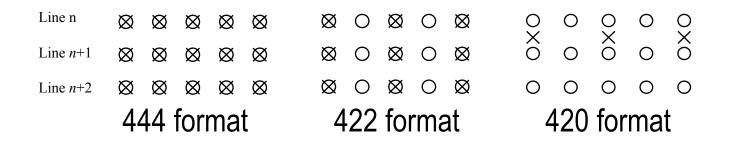






Chroma Sub-Sampling

- Chrominance information frequently needs to be sub-sampled in order to reduce processing, storage and transmission overhead.
- Commonly used sub-sampled chroma formats: 422 and 420.
- Conversion to 422 format requires only horizontal FIR filtering.
- Conversion to 420 format requires vertical interpolation between chrominance components as well



27







- The essence of embedded vision is applying sophisticated algorithms to image data
- Interfacing to image sensors is complex
- Implementing sophisticated algorithms on real-time video data is challenging
- FPGAs and FPGA-processor combinations address the key challenges for these applications
 - Flexible / High Speed Interfaces
 - Physical connection
 - Data formats
 - Serial, Parallel, Standard (LVDS, HDMI, MIPI, etc.)
 - Multiple Data Formats
 - Logic resources for flexible parallel processing
 - Design resources to support embedded vision applications
 - RTL, DSP, Embedded, High Level Synthesis flows
 - Library of intellectual property cores (IP)





The Embedded Vision Alliance Free Resources on Embedded Computer Vision

The Embedded Vision Alliance web site, at <u>www.Embedded-Vision.com</u>, covers embedded vision applications and technology, including interviews and demonstrations

Register on the Alliance web site for free access to:

- The Embedded Vision Academy—free in-depth tutorial articles, video "chalk talks," code examples, and discussion forums.
- Embedded Vision Insights—bimonthly newsletter with industry news and updates on new resources available on the Alliance website.

Embedded vision technology and services companies interested in becoming sponsoring members of the Alliance may contact info@Embedded-Vision.com











Embedded Vision Insights The Latest Developments on Designing Machines that See





Embedded Vision Summit

A Free Educational Event for Engineers—San Jose, April 25th

Learn how to use the hottest new technology in the industry to create "machines that see"

- Technical presentations on sensors, processors, tools, and design techniques
- Keynote by Prof. Pieter Abbeel, UC Berkeley, a leader in developing machine intelligence
- Cool demonstrations and opportunities to meet with leading vision technology suppliers



Co-located with UBM Electronics' DESIGN West

 DESIGN West also includes the Embedded Systems Conference, Black Hat Summit, and exhibits

The Summit is free, but space is limited. To register to attend, go to <u>www.embedded-vision.com/embedded-vision-summit</u>

30











Interfacing to and Processing Data from Image Sensors

March 19th 2013 Jose Roberto Alvarez Engineering Director Xilinx, Inc



