Designing a Robust IIoT to SCADA Gateway

Class 2: Introduction to the RZ/N1

October 23, 2018

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CEC CONTINUING EDUCATION CENTER

Digi-Key ELECTRONICS

This Week's Agenda

10/22 The Challenges of IIoT and Industrial Ethernet

10/23 Introduction to the RZ/N1

10/24 Many Protocols, One Abstraction - GOAL

10/25 Programming the R-IN Protocol Engine

10/26 Writing and Testing Our Application

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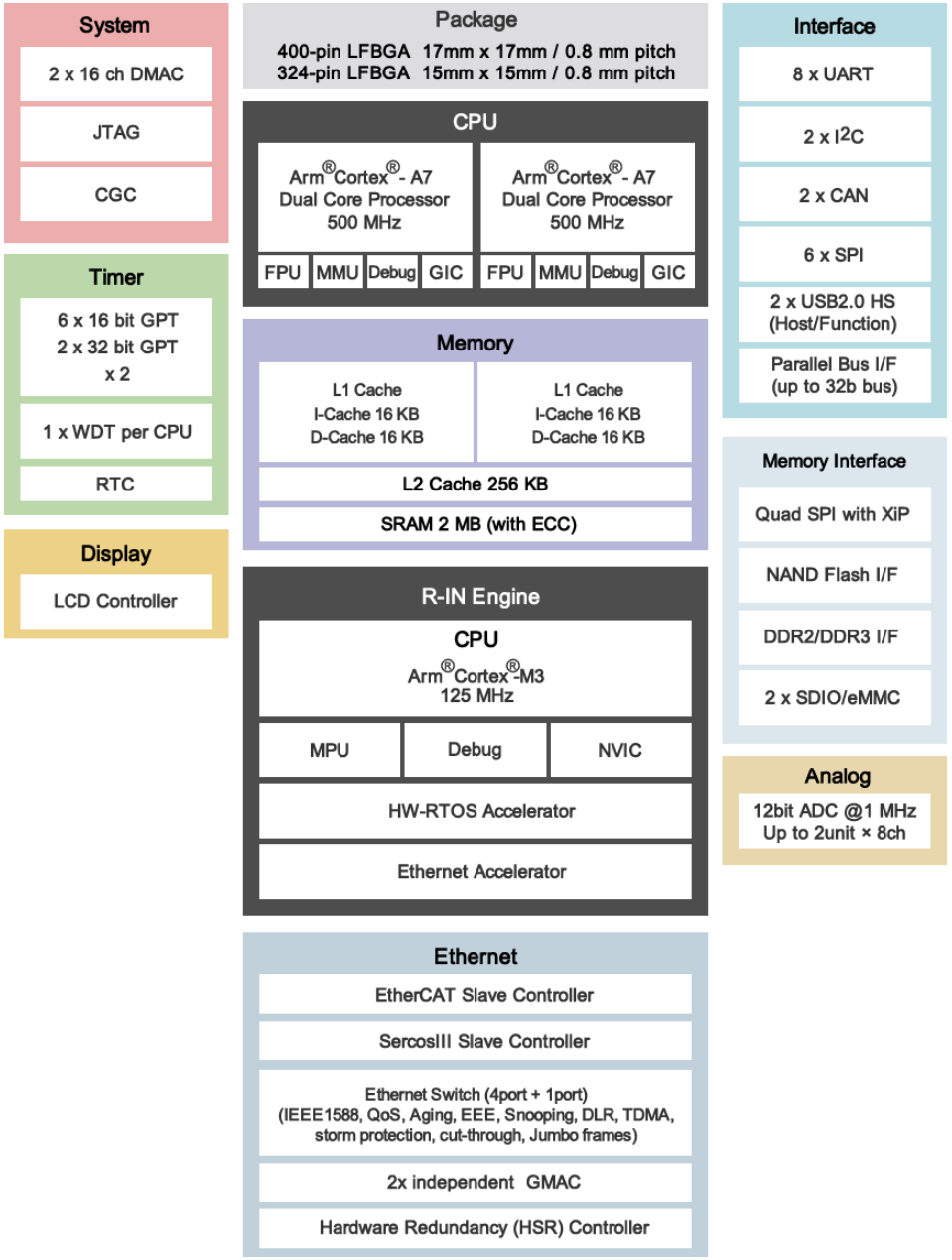
Many Protocols, One Chip

- Yesterday we saw that we need to be able to interface with many different protocols, some of which have specific hardware requirements
- Today we will look at the Renesas RZ/N1 family of processors, particularly the RZ/N1D with dual ARM Cortex A7 application processors.


System
2 x 16 ch DMAC
JTAG
CGC
Timer
6 x 16 bit GPT
2 x 32 bit GPT
x 2
1 x WDT per CPU
RTC
Display
LCD Controller
Package
400-pin LFBGA 17mm x 17mm / 0.8 mm pitch
324-pin LFBGA 15mm x 15mm / 0.8 mm pitch
CPU
Arm®Cortex®- A7
Dual Core Processor
500 MHz
FPU MMU Debug GIC
Arm®Cortex®- A7
Dual Core Processor
500 MHz
FPU MMU Debug GIC
Memory
L1 Cache
I-Cache 16 KB
D-Cache 16 KB
L1 Cache
I-Cache 16 KB
D-Cache 16 KB
L2 Cache 256 KB
SRAM 2 MB (with ECC)
R-IN Engine
CPU
Arm®Cortex®-M3
125 MHz
MPU
Debug
NVIC
HW-RTOS Accelerator
Ethernet Accelerator
Ethernet
EtherCAT Slave Controller
SercosIII Slave Controller
Ethernet Switch (4port + 1port)
(IEEE1588, QoS, Aging, EEE, Snooping, DLR, TDMA,
storm protection, cut-through, Jumbo frames)
2x independent GMAC
Hardware Redundancy (HSR) Controller
Interface
8 x UART
2 x I2C
2 x CAN
6 x SPI
2 x USB2.0 HS
(Host/Function)
Parallel Bus I/F
(up to 32b bus)
Memory Interface
Quad SPI with XiP
NAND Flash I/F
DDR2/DDR3 I/F
2 x SDIO/eMMC
Analog
12bit ADC @1 MHz
Up to 2unit × 8ch

R-IN Engine Ethernet

- EtherSwitch (4port + 1port)
  - QoS, Aging, EEE, Snooping, DLR, TDMA, Storm protection cut through, Jumbo frames
- Ethernet hardware acceleration
- EtherCAT slave controller
- Sercos® III slave controller
- HSR switch (in 400-pin package)
- 5-port Ethernet switch

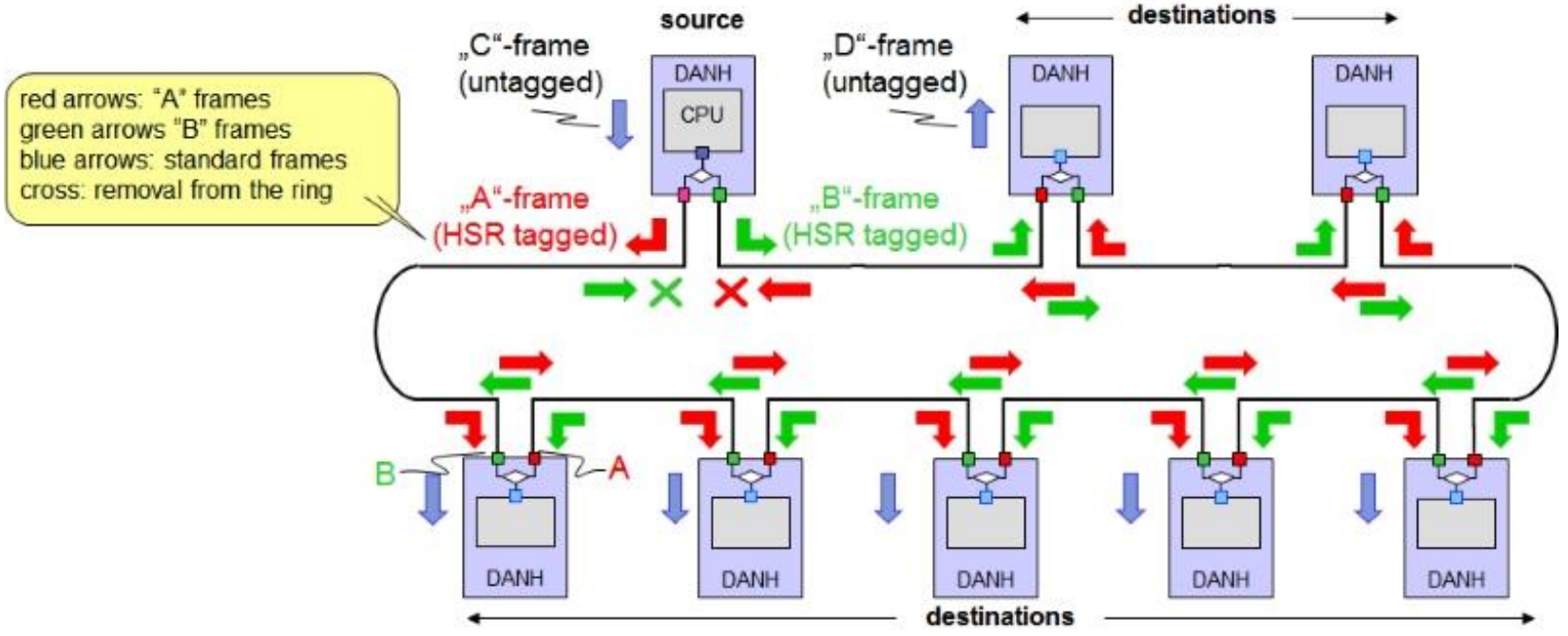
Question 1– What does storm protection do?

Energy-Efficient Ethernet

- IEEE 802.3az
- Establishes a protocol for powering down the PHY transmitter during lulls in transmission
- Significant power savings, less heat dissipation

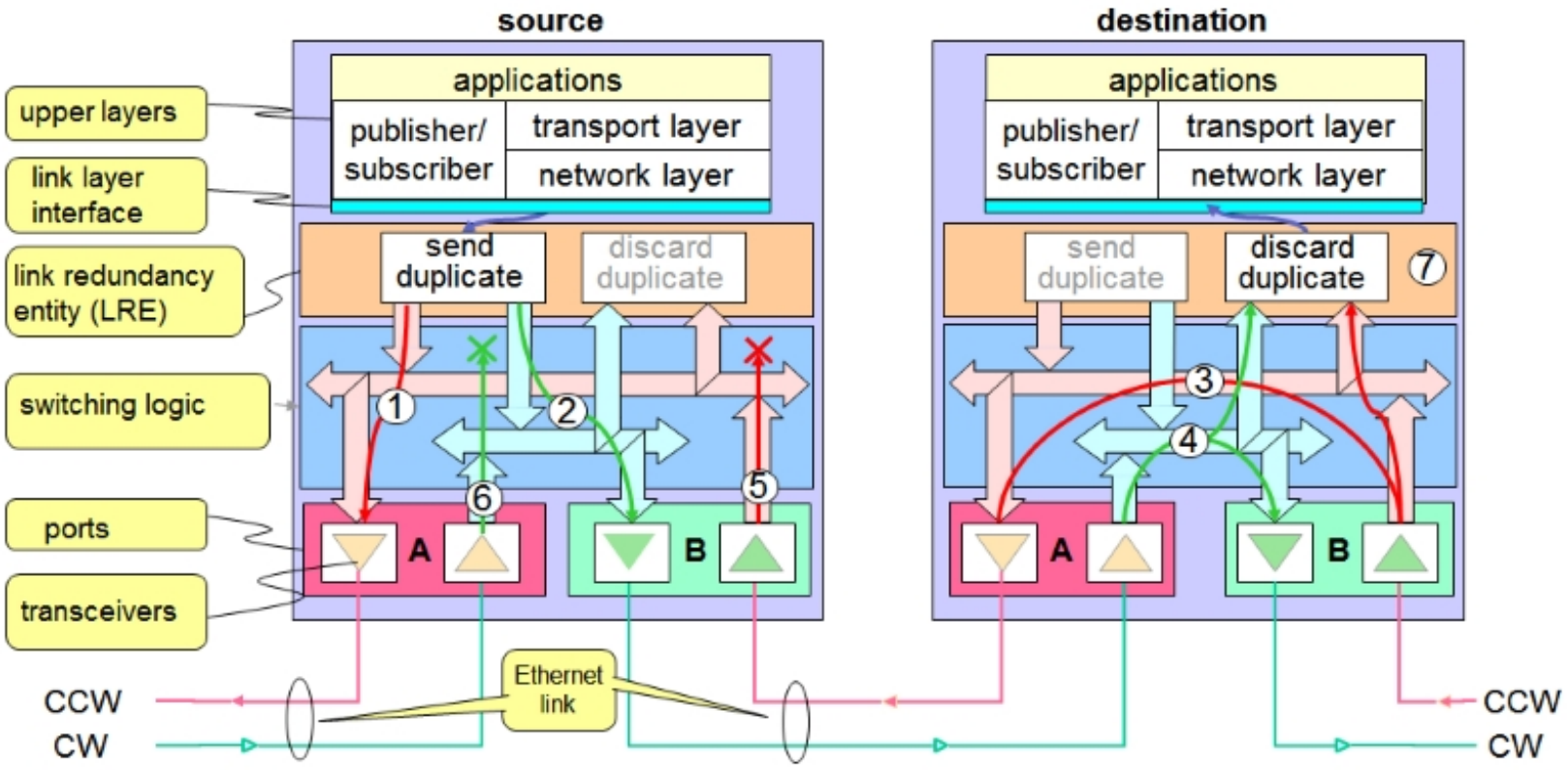
Energy Efficient Ethernet

High-availability Seamless Redundancy (HSR)



HSR is built on a Device Level Ring (DLR) structure

HSR Detail


source
destination
upper layers
link layer interface
link redundancy entity (LRE)
switching logic
ports
transceivers
applications
publisher/ subscriber
transport layer
network layer
send duplicate
discard duplicate
1
2
3
4
5
6
7
A
B
Ethernet link
CCW
CW
CCW
CW

Other I/O

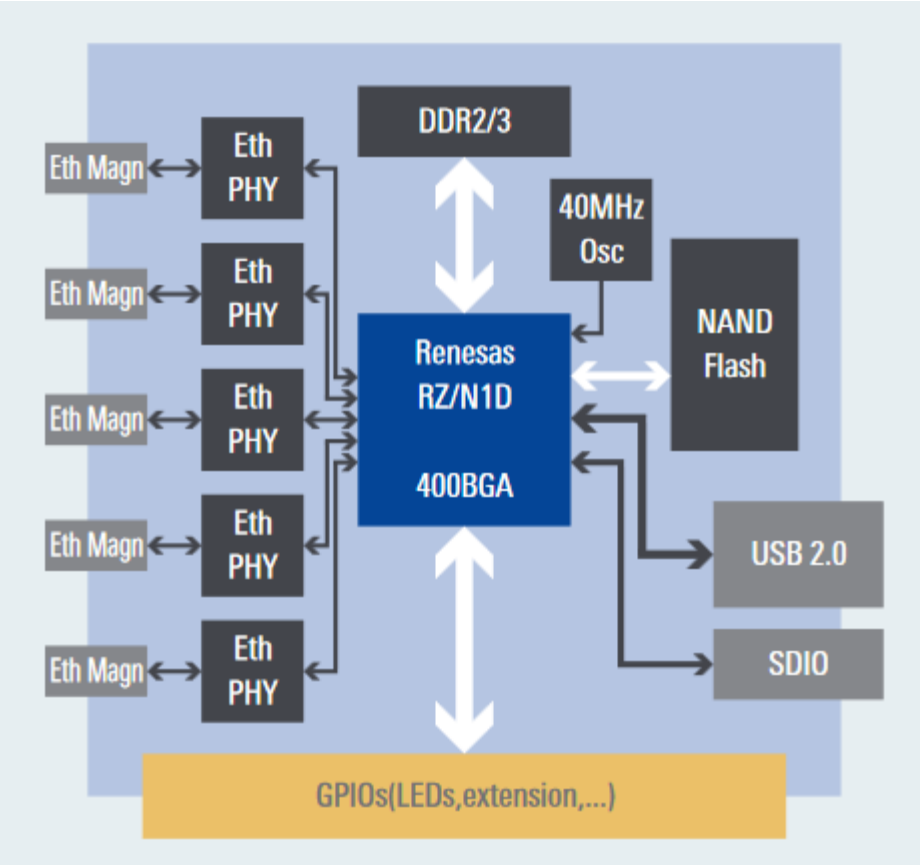
- UART × 8 channels
- I^2C × 2 channels
- USB Host (HS)
- SPI × 6 channels (4 master, 2 slave)
- CAN bus
- LCD controller
- ADC: 12-bit × 8 channels (2 units in 400pin)
- GPIO and Parallel bus

R-IN Communication

- µITRON-like system calls
  - 30 system calls for elements such as events, semaphores, and mailboxes
- Task Scheduler
  - Hardware ISR: 32 routines selectable from 128 QINT routines
  - Number of context elements: 64
  - Number of semaphore identifiers: 128
  - Number of event identifiers: 64
  - Number of mailbox identifiers: 64
  - Number of mailbox elements: 192
  - Number of context priority levels: 16

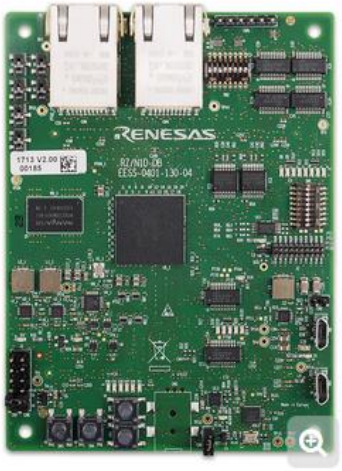
Question 2 – What is the difference between ITRON and µITRON?

Example - PLC


DDR2/3
Eth Magn
Eth PHY
Eth Magn
Eth PHY
Eth Magn
Eth PHY
Eth Magn
Eth PHY
Eth Magn
Eth PHY
40MHz Osc
Renesas RZ/N1D
400BGA
NAND Flash
USB 2.0
SDIO
GPIOs(LEDs,extension,...)

RZ/N1 Boards

Dual Cortex-A7



RZ/N1D CPU Board

Single Cortex-A7

RZ/N1S CPU Board

R-IN Engine

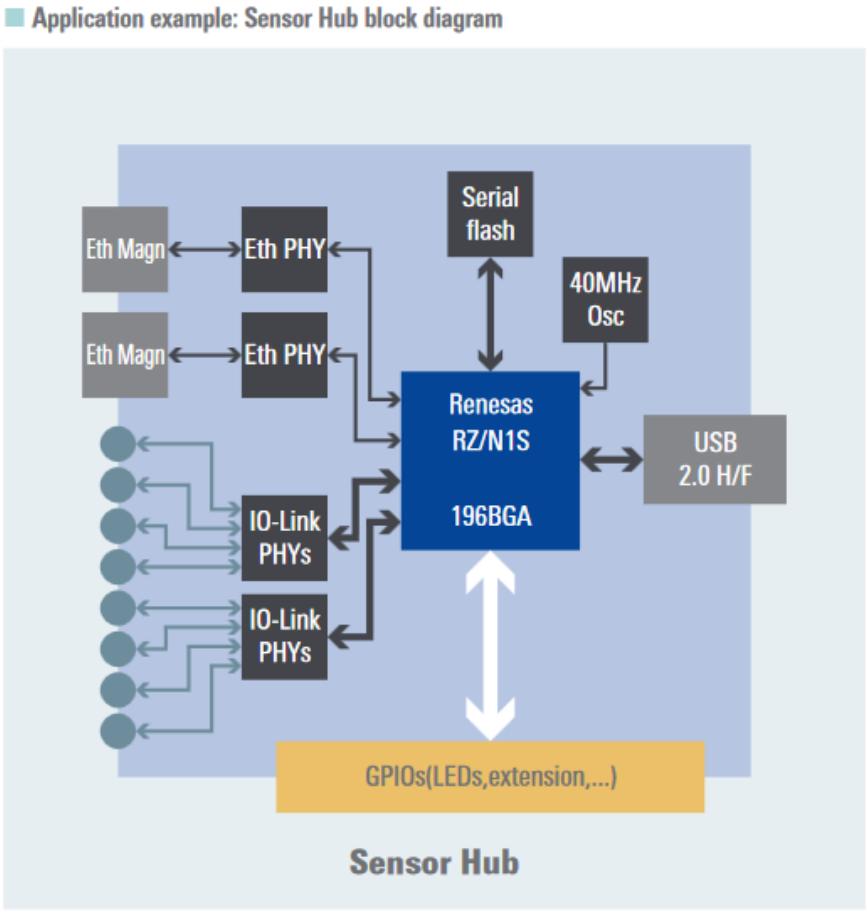
RZ/N1L CPU Board

Expansion Board

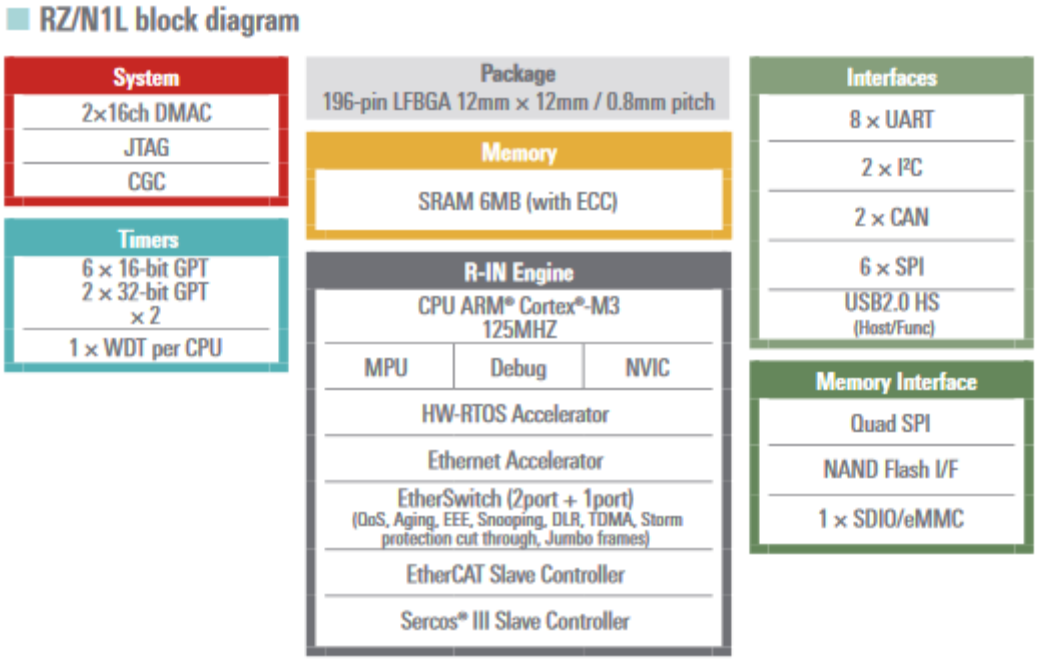
RZ/N1 Expansion Board

Example – Hub or Gateway

Note – single Cortex A7 Processor



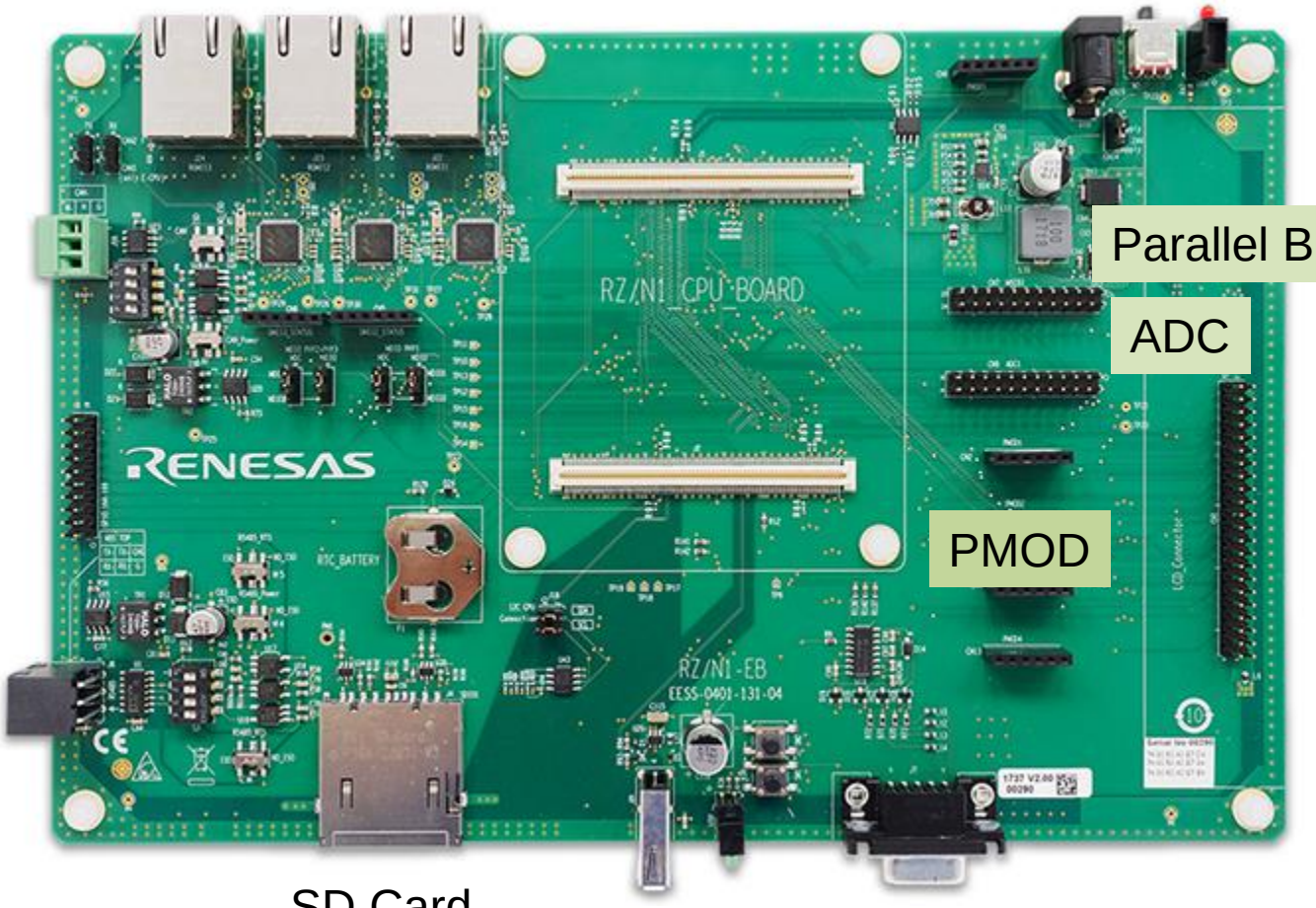
RZ/N1L (R-IN Stand Alone)



Development Board

- Basic CONNECT-IT! Kit
- RZ/N1D Board
- IAR I-jet Lite JTAG
- DVD with software, manuals
- Cables
- Available for loan from your Renesas office

Expansion Board



Developing With the RZ/N1D

- Treat as two entities:
  - Application Processor (Dual ARM Cortex-A7)
  - Communications Processor (ARM Cortex-M3)
- Application Processor can either be programmed with an RTOS or with a full O/S (Linux – preferred)
- Communications processor is programmed with an RTOS
- Code is provided for both Linux (including a port) and baremetal / RTOS
- More on this Thursday and Friday!

Industrial Ethernet Stacks

RZ/N Series: Solutions from Renesas Partners

A variety of software solutions are available from vendors with deep expertise in industrial networks.

Protocol Vendor	
Port.GmbH	Industrial network stack PROFINET (Slave) EtherNet/IP (Slave) Powerlink (Slave)
TMG (TMG Technologie und Engineering GmbH)	Industrial network stack PROFINET (Slave) EtherNet/IP (Slave)
Cannon Automata	Industrial network stack Sercos® III (Slave)
NetModule	Redundant protocol HSR/PRP

Available Development Environments

RZ/N Series: Development Environments

	IAR SYSTEMS	WIND	RENESAS
CPU Core	• Cortex®-A7 • Cortex®-M3	• Cortex®-A7 (for VxWorks)	• Cortex®-A7 (for Linux)
Debugger	• Embedded • Workbench	• Eclipse	• GDB
Compiler	• IAR • C/C++Compiler	• GCC • DIAB	• GCC
ICEs	• I-jet™	• JTAG debugger (LAUTERBACH)	• J-Link (SEGGER)

Question 3 – What popular board uses Cortex A7 cores (and typically Linux)?

Common Abstraction

- Programming our ports to accommodate all of these protocols needs a common abstraction layer
- The Renensas RZ/N1D R-IN protocol engine makes use of the GOAL (Generic Open Abstraction Layer) from PORT GmbH in order to make our programming more straightforward
- More on this tomorrow!

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Please stick around as I answer your questions!

- Please give me a moment to scroll back through the chat window to find your questions
- I will stay on chat as long as it takes to answer!
- I am available to answer simple questions or to consult (or offer in-house training for your company)
  c.j.lord@ieee.org
  http://www.blueridgetechnc.com
  http://www.linkedin.com/in/charleslord
  Twitter: @charleslord
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