



DesignNews

Field-Programmable Gate Array (FPGA) Primer

Day 3: Vivado Simulation

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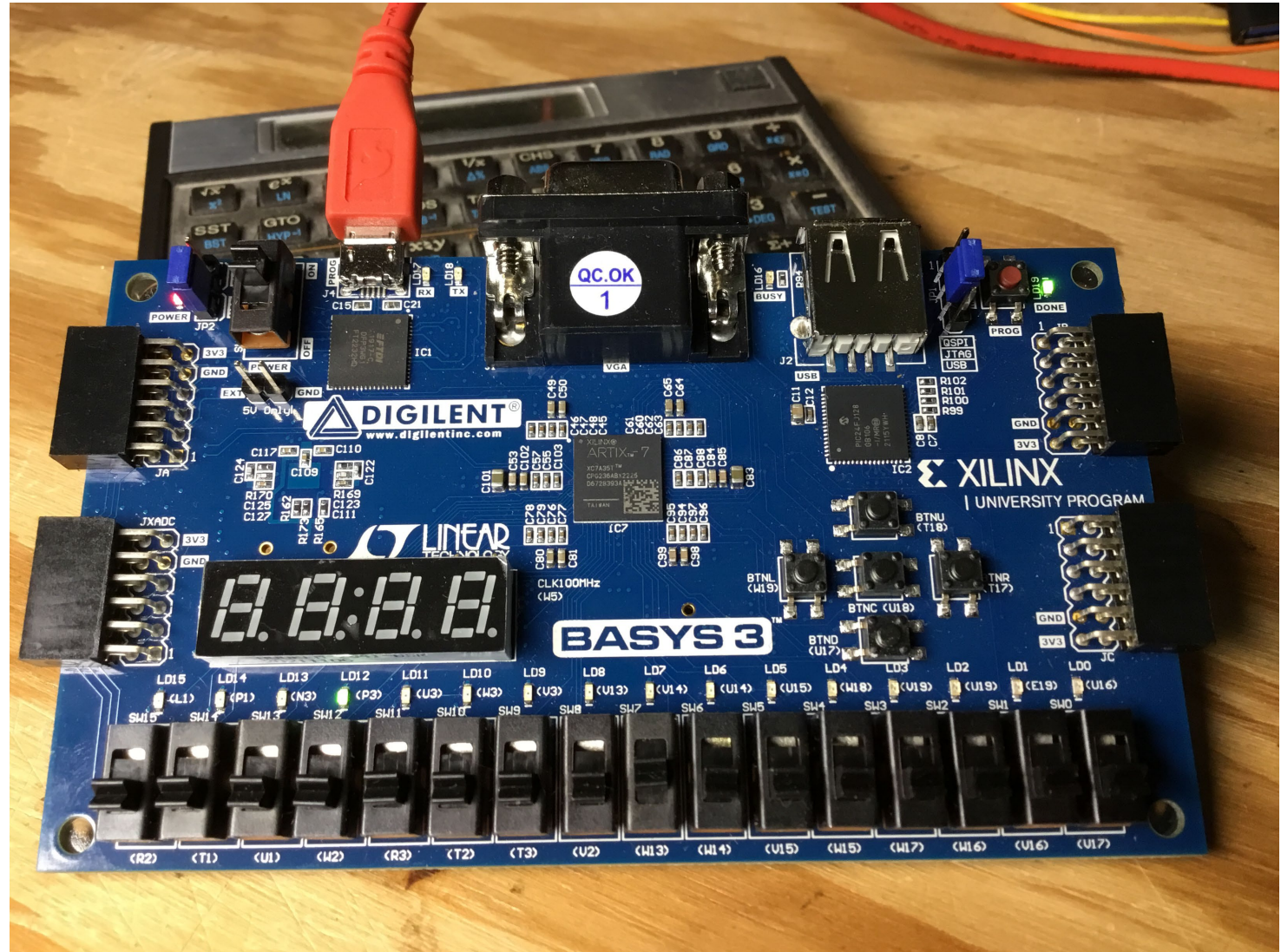
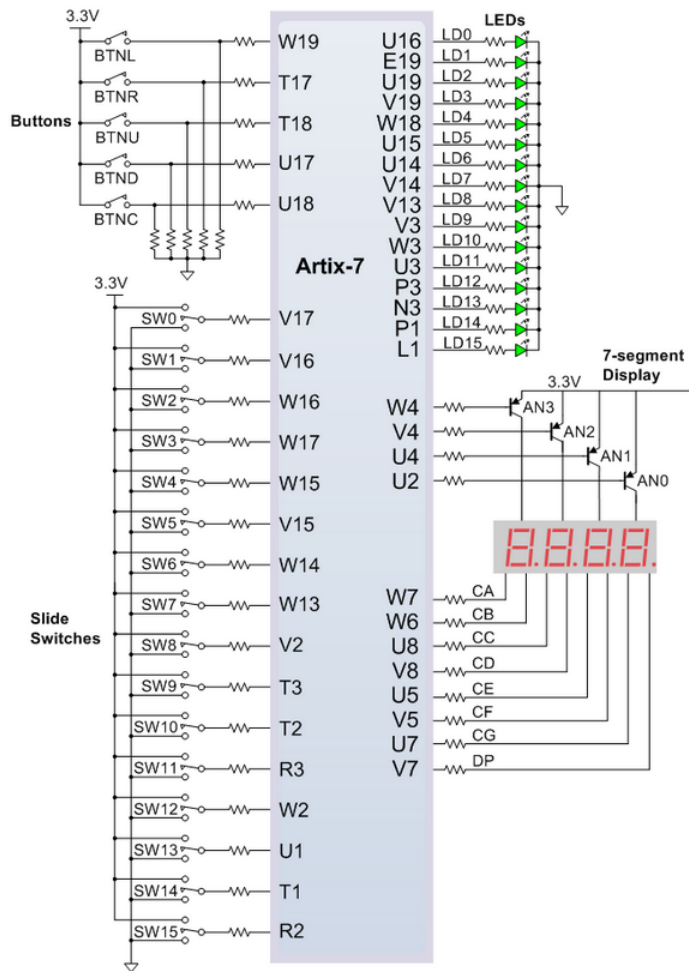


Fred Eady

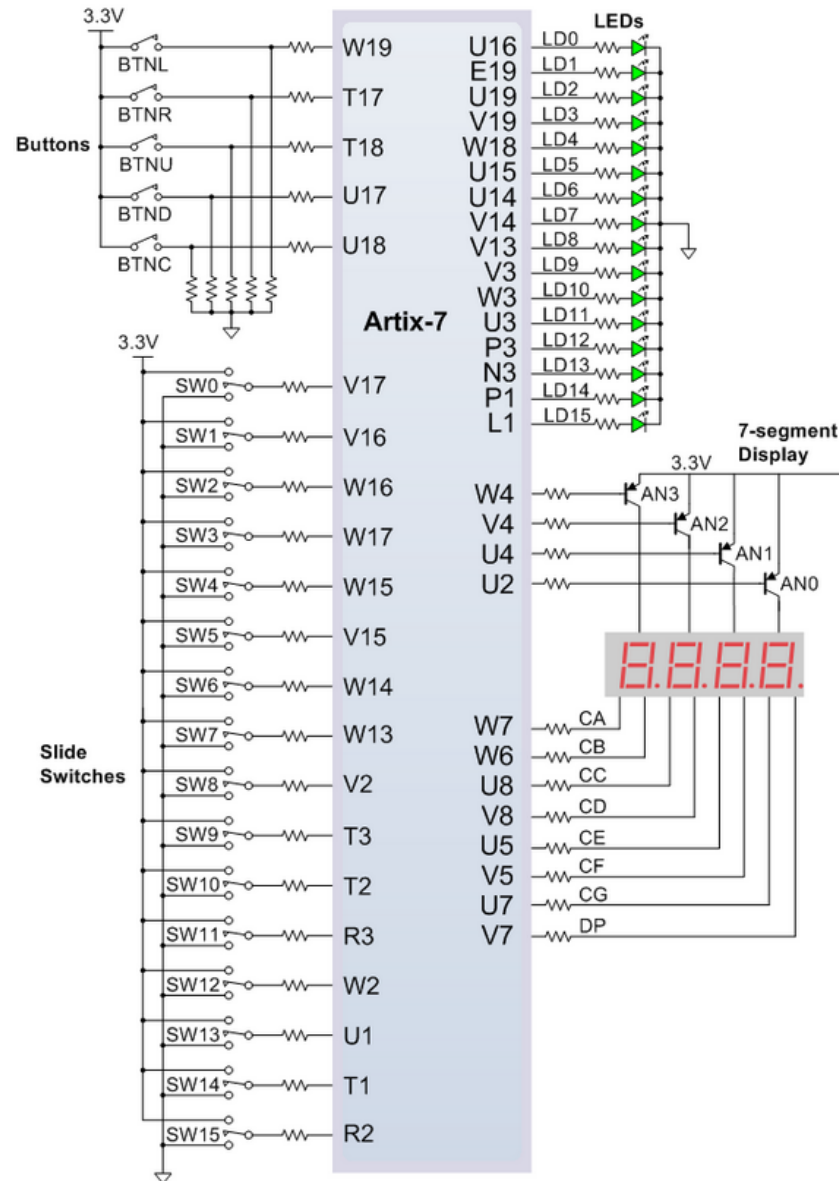
Visit 'Lecturer Profile' in your console for more details.

AGENDA

- **Simulation by Force**
- **Simulation by Code**



Simulation Sources – debounce_top



The screenshot shows the PROJECT MANAGER interface for a project named 'debounce_A'. The 'Sources' list is expanded to show the 'debounce_top' component. A red arrow points to the 'Run Simulation' button in the left-hand pane.

Flow Navigator

- > PROJECT MANAGER
- > IP INTEGRATOR
- ▼ SIMULATION
 - Run Simulation
- > RTL ANALYSIS
- > SYNTHESIS
- > IMPLEMENTATION
- > PROGRAM AND DEBUG

PROJECT MANAGER - debounce_A

Sources

- Design Sources (1)
 - > ● **debounce_top** (debounce_top.v) (4)
- Constraints (1)
 - >
- Simulation Sources (1)
 - ▼ sim_1 (1)
 - ▼ ● **debounce_top** (debounce_top.v) (4)
 - dbclk_enable : dbnc_clk (dbnc_clk.v)
 - dff0 : d_flipflop_en (d_flipflop_en.v)
 - dff1 : d_flipflop_en (d_flipflop_en.v)
 - dff2 : d_flipflop_en (d_flipflop_en.v)
- Utility Sources (1)
 - >

Hierarchy Libraries Compile Order

Simulation Sources – debounce_top

The screenshot displays the simulation tool interface for a behavioral simulation of a debounce_top circuit. The interface is divided into several panels:

- Flow Navigator:** Shows the project structure with 'SIMULATION' selected.
- Scope:** A table listing simulation sources:

Name	Design Unit	B
debounce_top	debounce_top	V
dbclk_enable	dbnc_clk	V
dff0	d_flipflop_en	V
dff1	d_flipflop_en	V
dff2	d_flipflop_en	V
glbl	glbl	V

- Objects:** A table showing the current values of simulation objects:

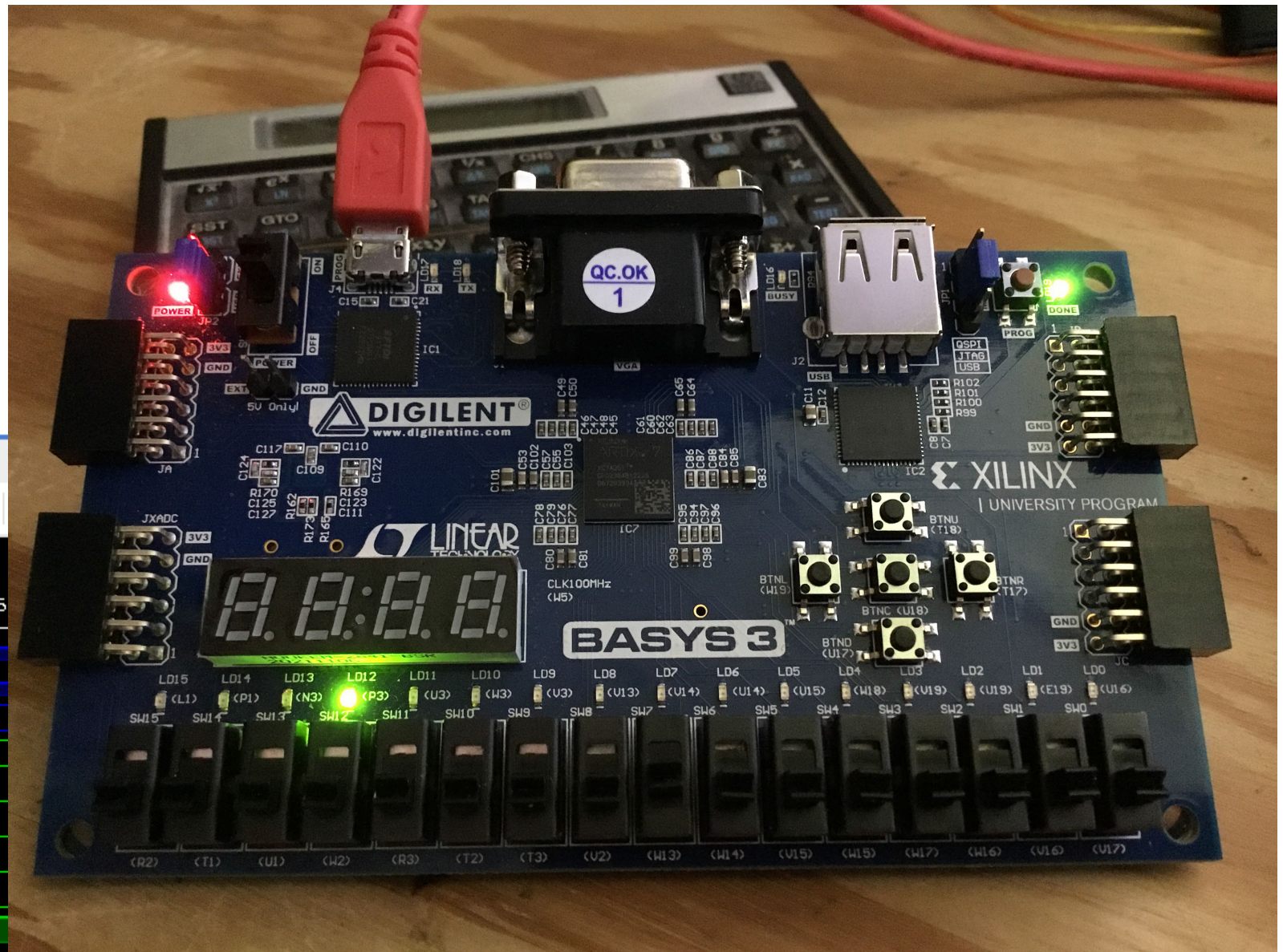
Name	Value	Data
clk	Z	Logic
dbnc_clk_out	0	Logic
counter[26:0]	0000000	Array

- Timing Diagram:** Shows a waveform for the simulation. The time axis is marked from 999,994 ps to 1,000,000 ps. The diagram shows signals for clk, btnC, led[15:0], an[3:0], w_clk_enable, w_Q0, w_Q1, w_Q2, and w_Q2_bar. A yellow vertical line is positioned at 1,000,000 ps.

Forced Simulation Setup – Initial Sim Run

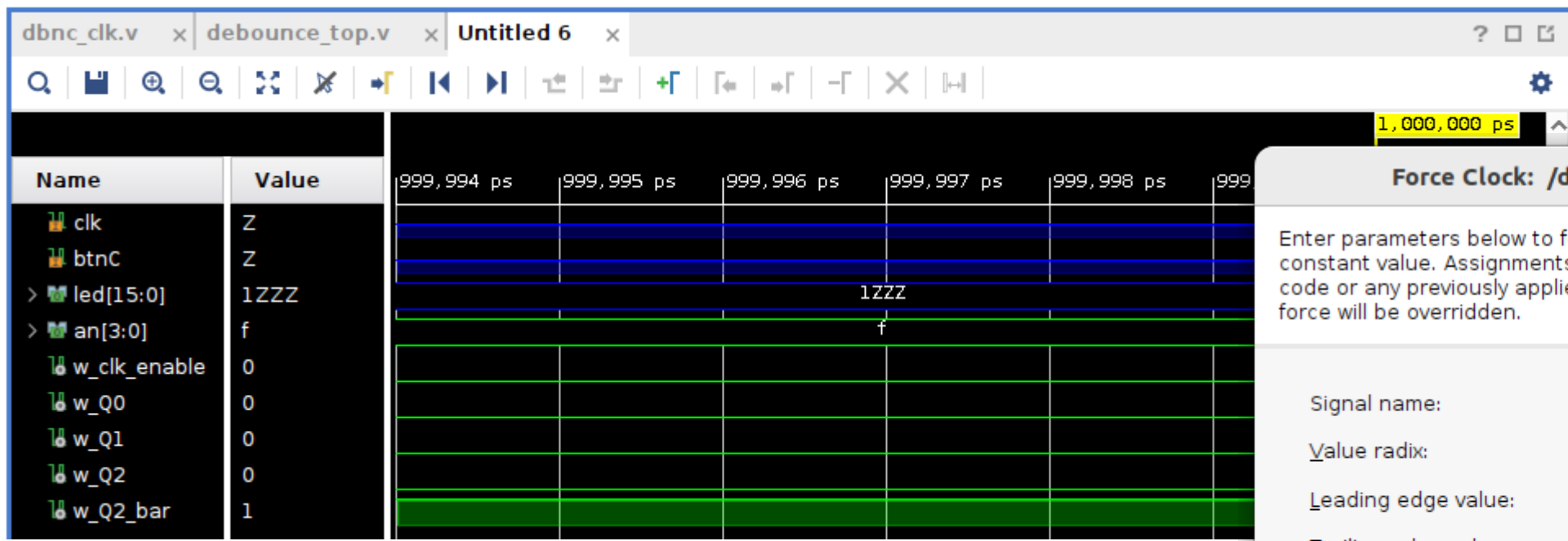
```

57 //led[1] on as long as btnC is depressed
58 assign led[1] = w_Q2;
59 //led[0] on for 1 second
60 assign w_Q2_bar = ~w_Q2;
61 assign led[0] = w_Q1 & w_Q2_bar;
62 assign led[15] = w_Q0;
63 assign led[14] = w_Q1;
64 assign led[13] = w_Q2;
65 assign led[12] = w_Q2_bar;
  
```



Name	Value
clk	Z
btnC	Z
led[15:0]	1ZZZ
an[3:0]	f
w_clk_enable	0
w_Q0	0
w_Q1	0
w_Q2	0
w_Q2_bar	1

Forced Simulation Setup – Force a Clock Signal



Force Clock: /debounce_top/clk

Enter parameters below to force the signal to a constant value. Assignments made from within HDL code or any previously applied constant or clock force will be overridden.

Signal name: /debounce_top/clk

Value radix:

Leading edge value:

Trailing edge value:

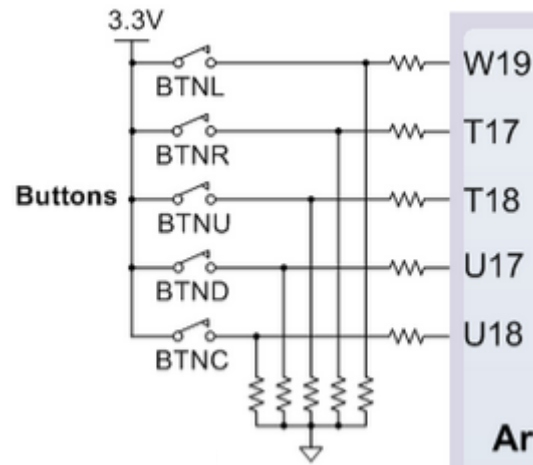
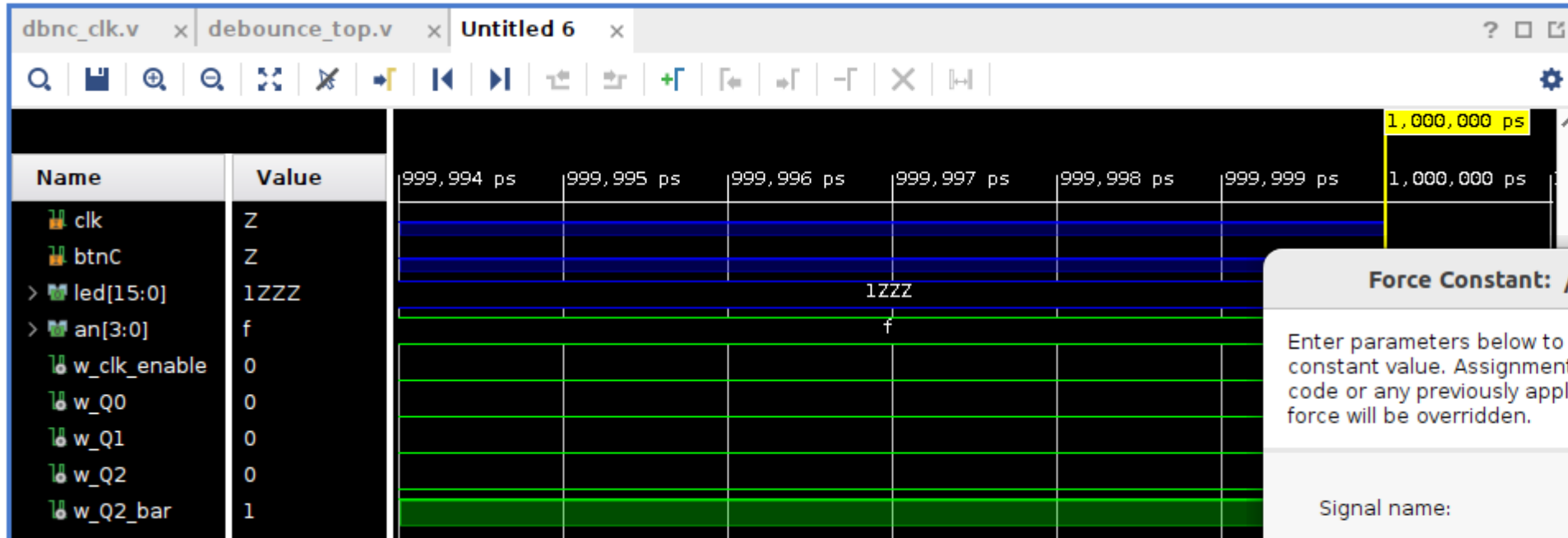
Starting after time offset:

Cancel after time offset:

Duty cycle (%):

Period: 100MHz clock

Forced Simulation Setup – Force a Sim Button Push



Force Constant: /debounce_top/btnC

Enter parameters below to force the signal to a constant value. Assignments made from within HDL code or any previously applied constant or clock force will be overridden.

Signal name: /debounce_top/btnC

Value radix: Hexadecimal

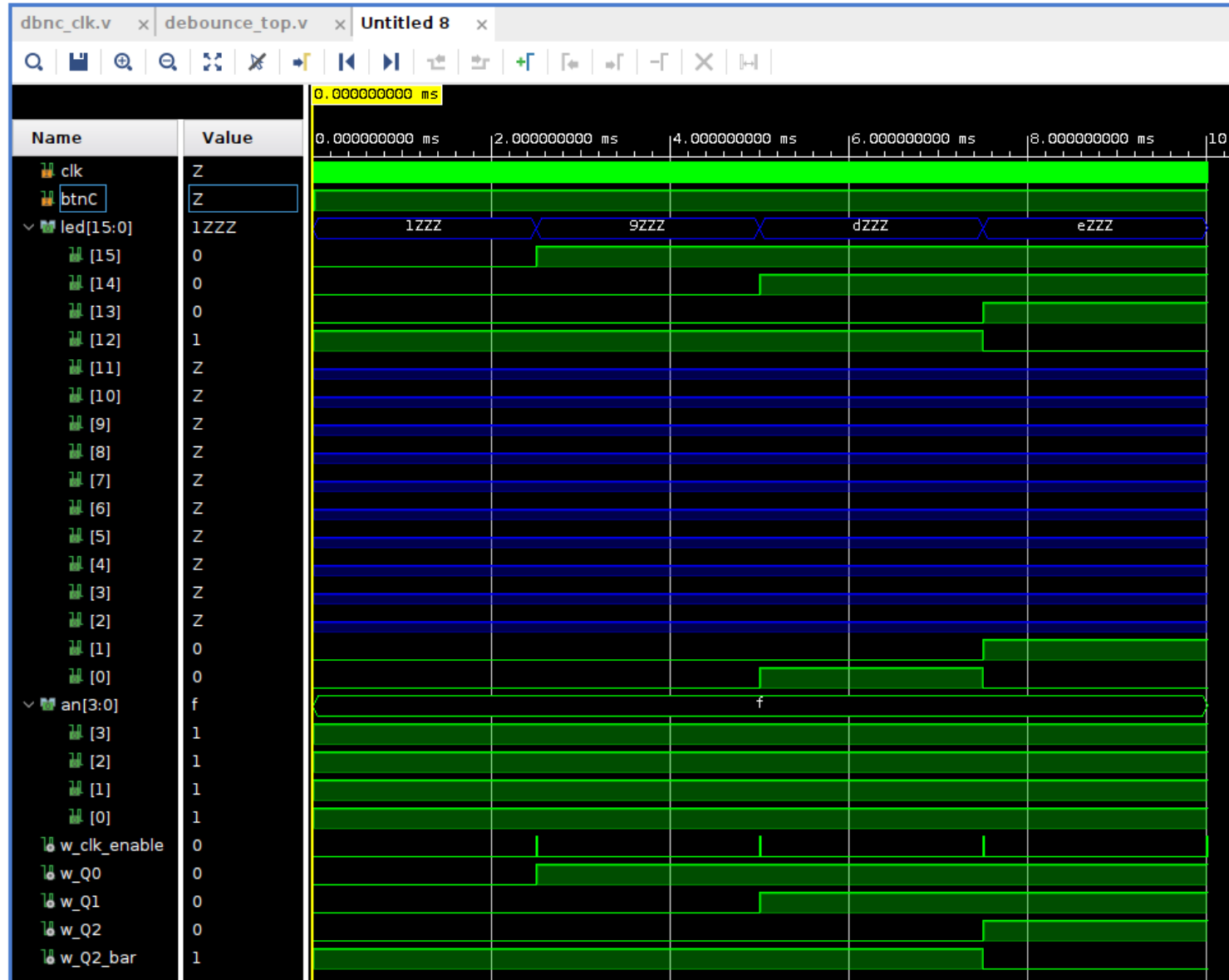
Force value: 1

Starting after time offset: 100ns

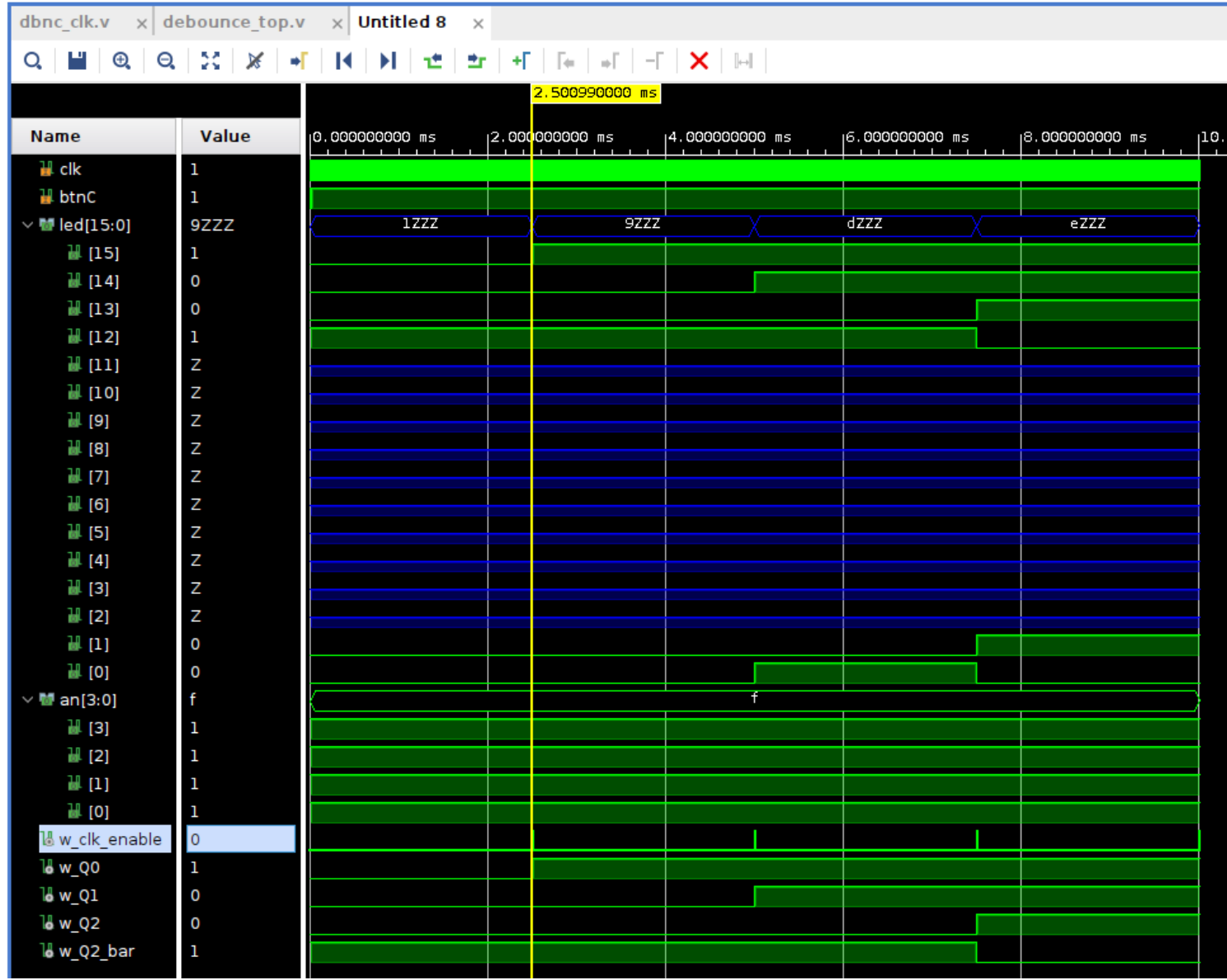
Cancel after time offset:

OK Cancel

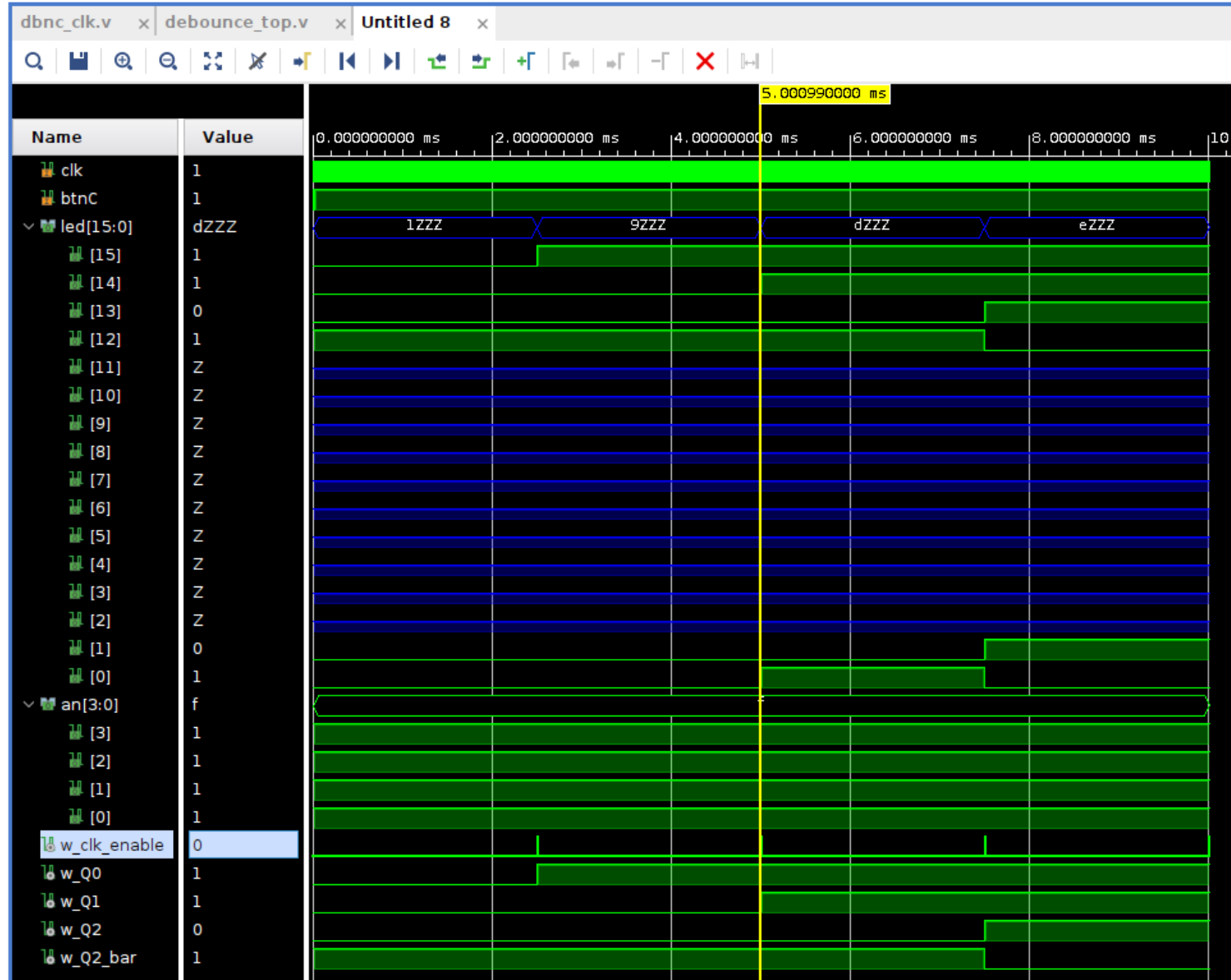
Forced Simulation Run – 10mS



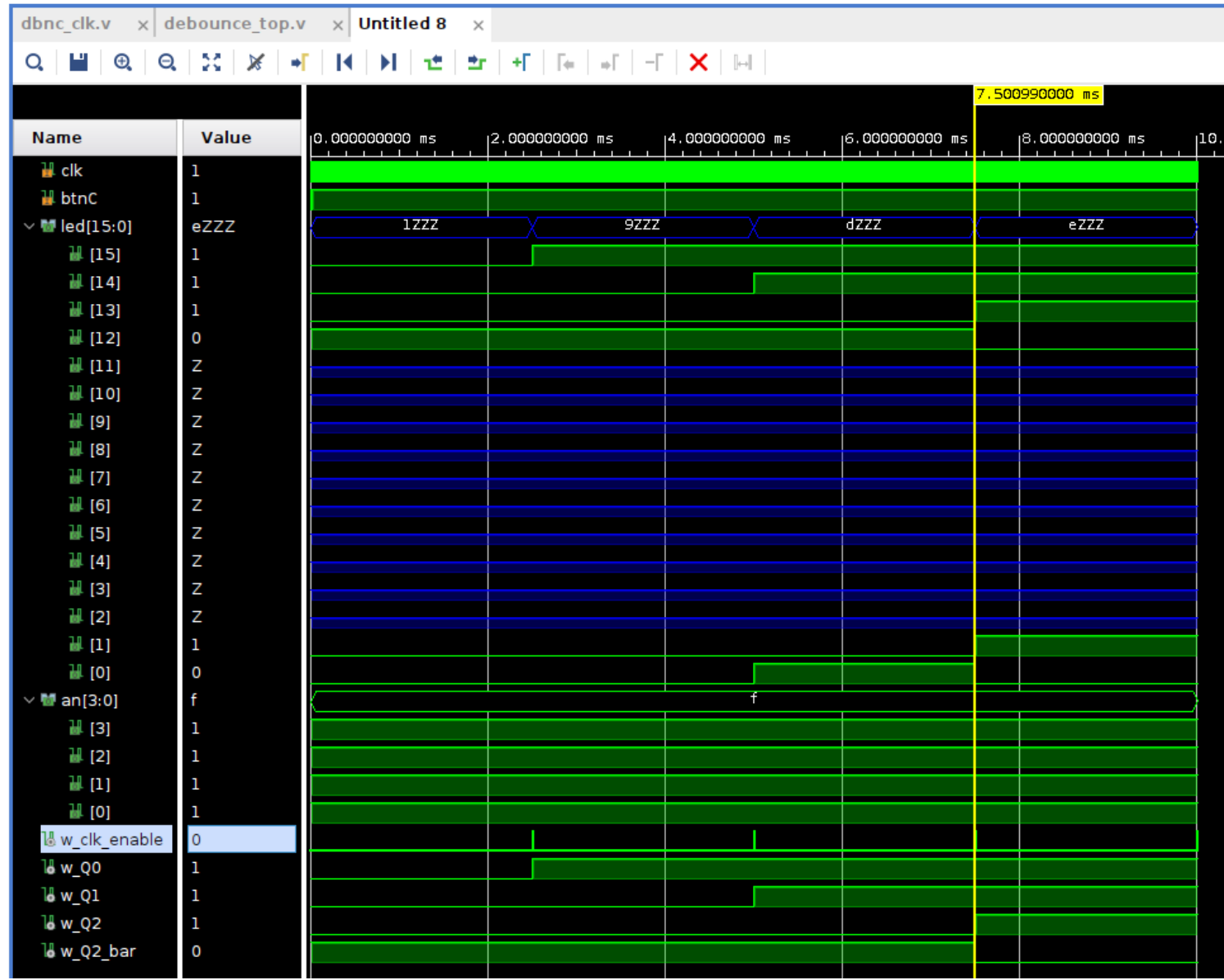
Forced Simulation Run – clk enable pulse 1



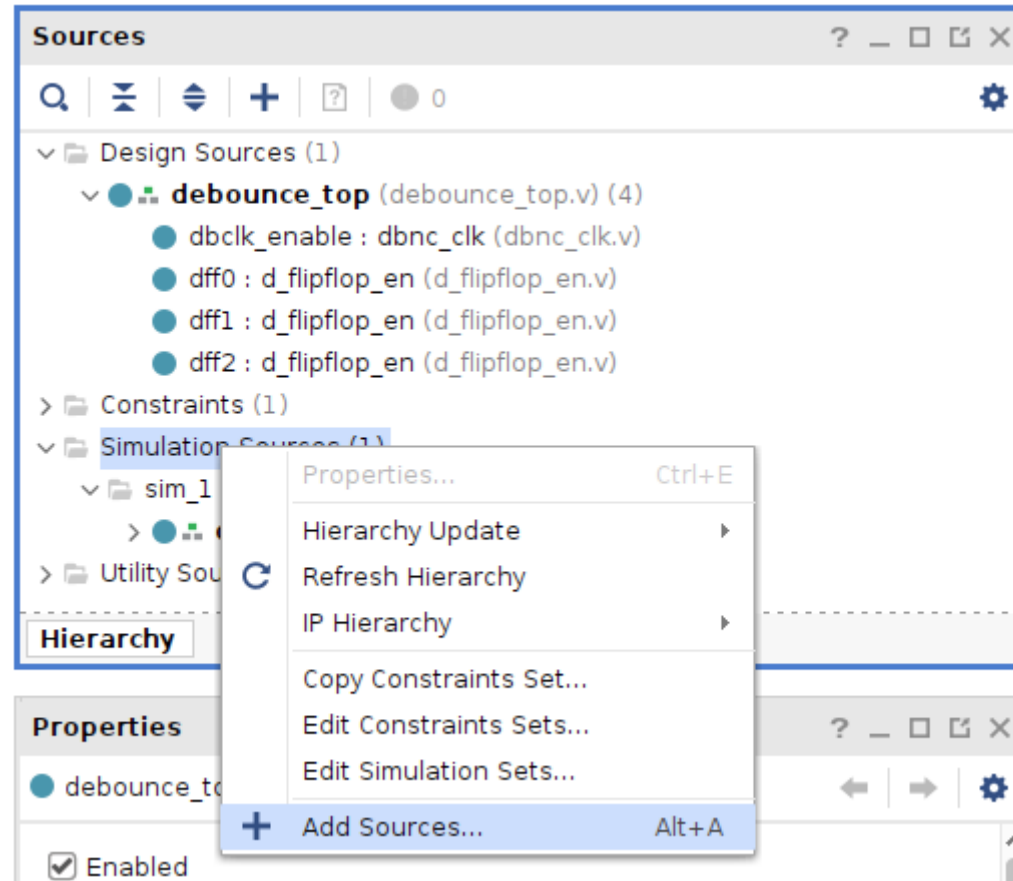
Forced Simulation Run – clk enable pulse 2



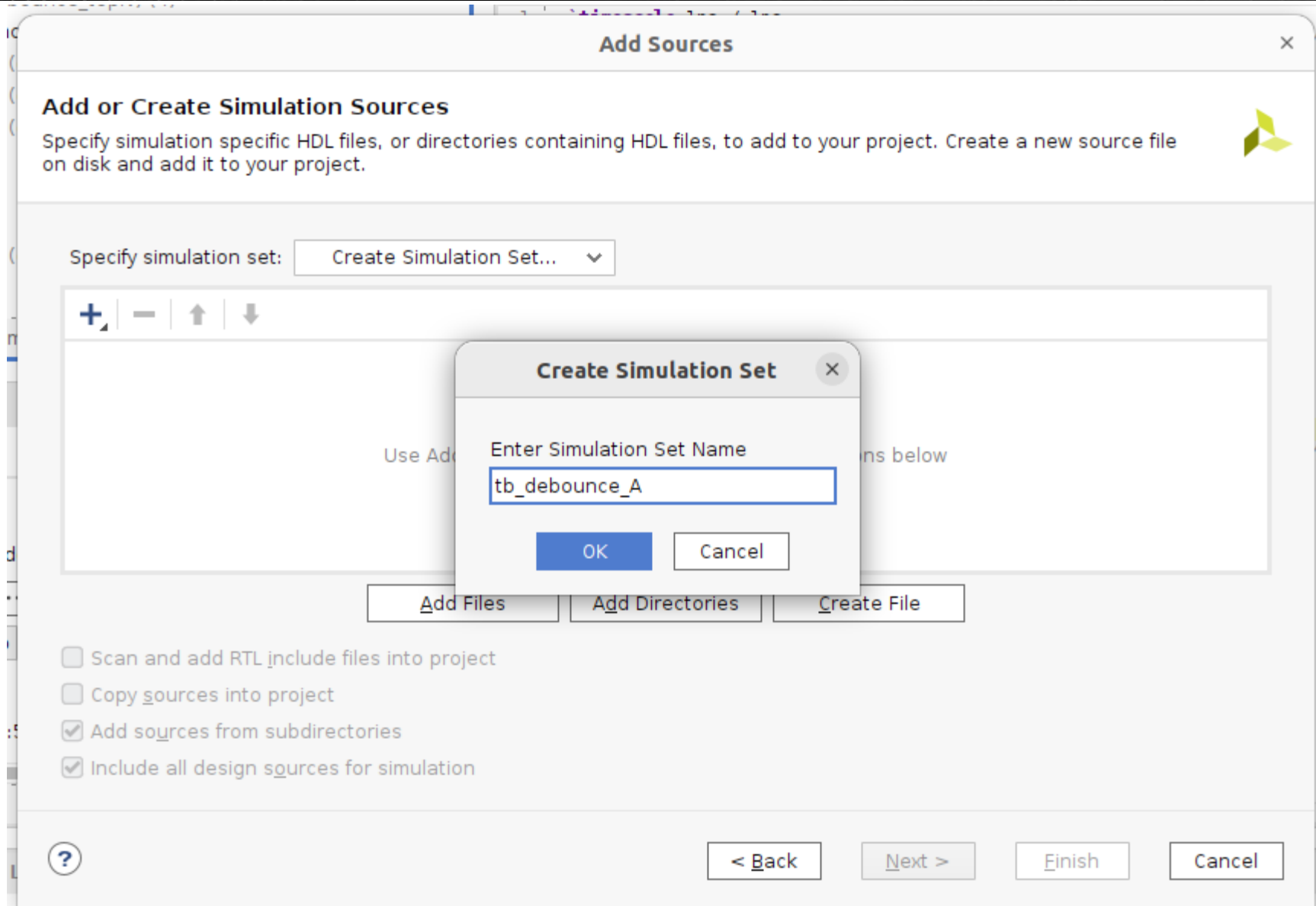
Forced Simulation Run – clk enable pulse 3



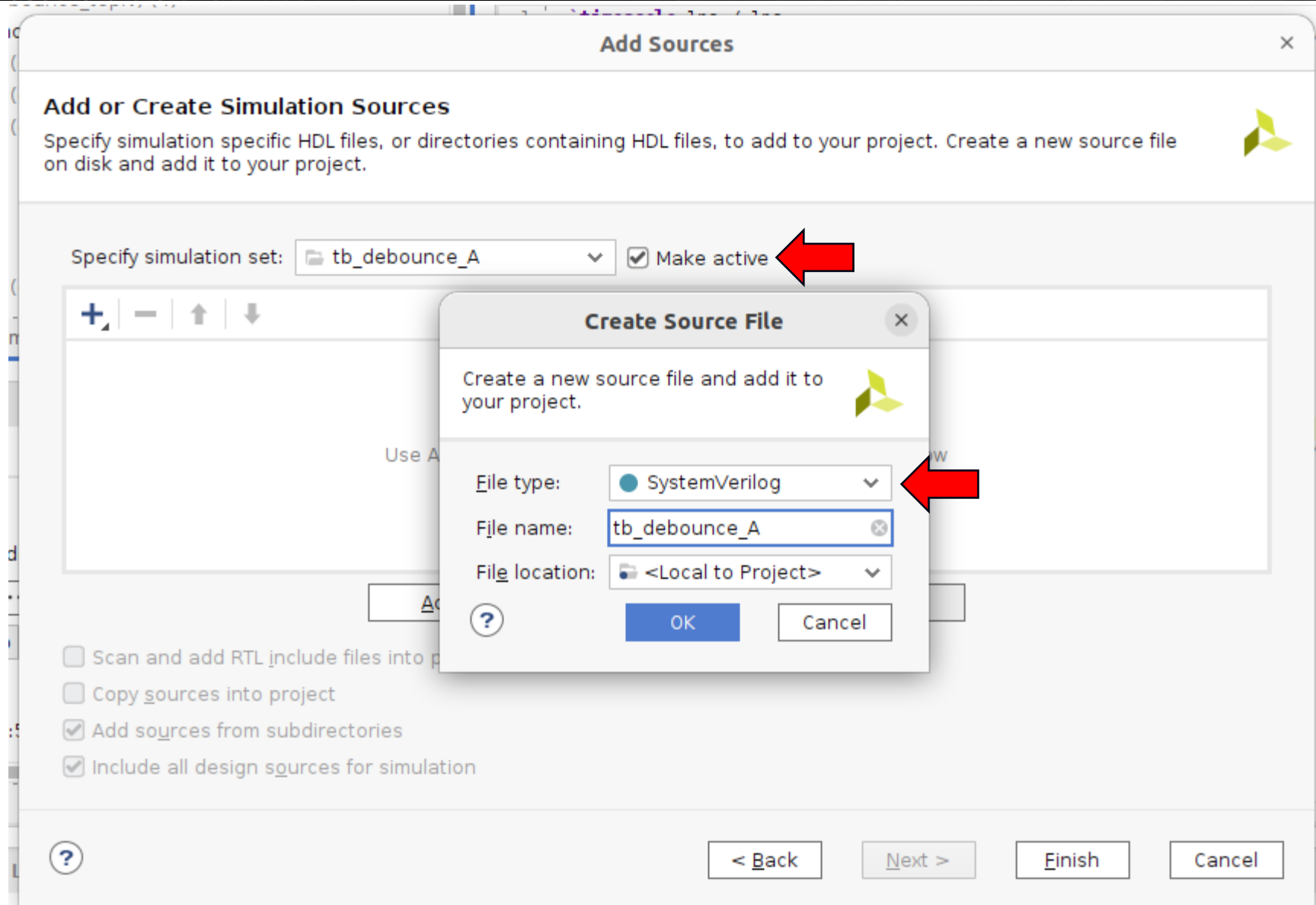
Coded Simulation Setup



Coded Simulation Setup



Coded Simulation Setup



Coded Simulation Setup

Define Module


Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

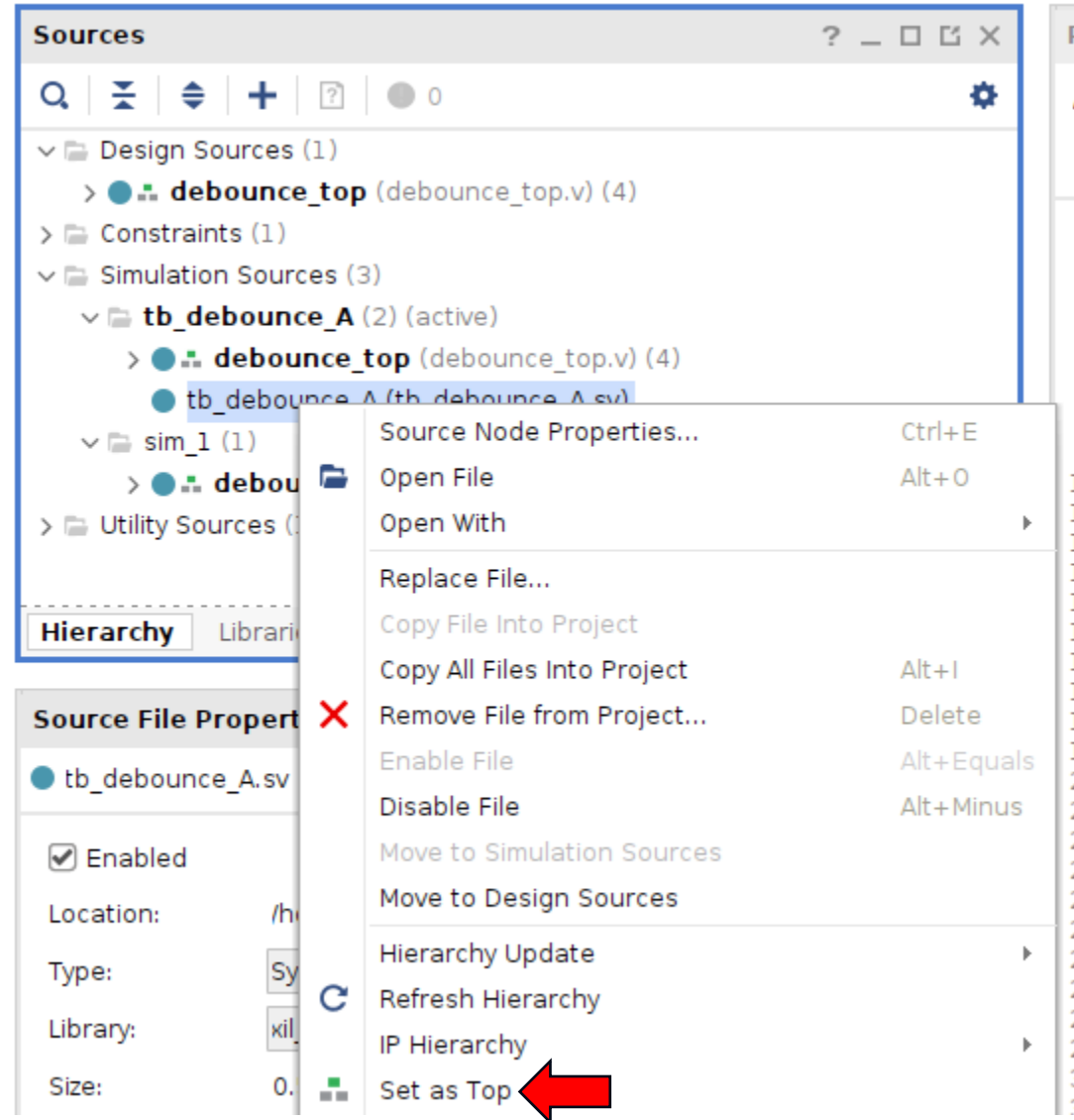
Module name:

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
	input	<input type="checkbox"/>	0	0



Coded Simulation Setup

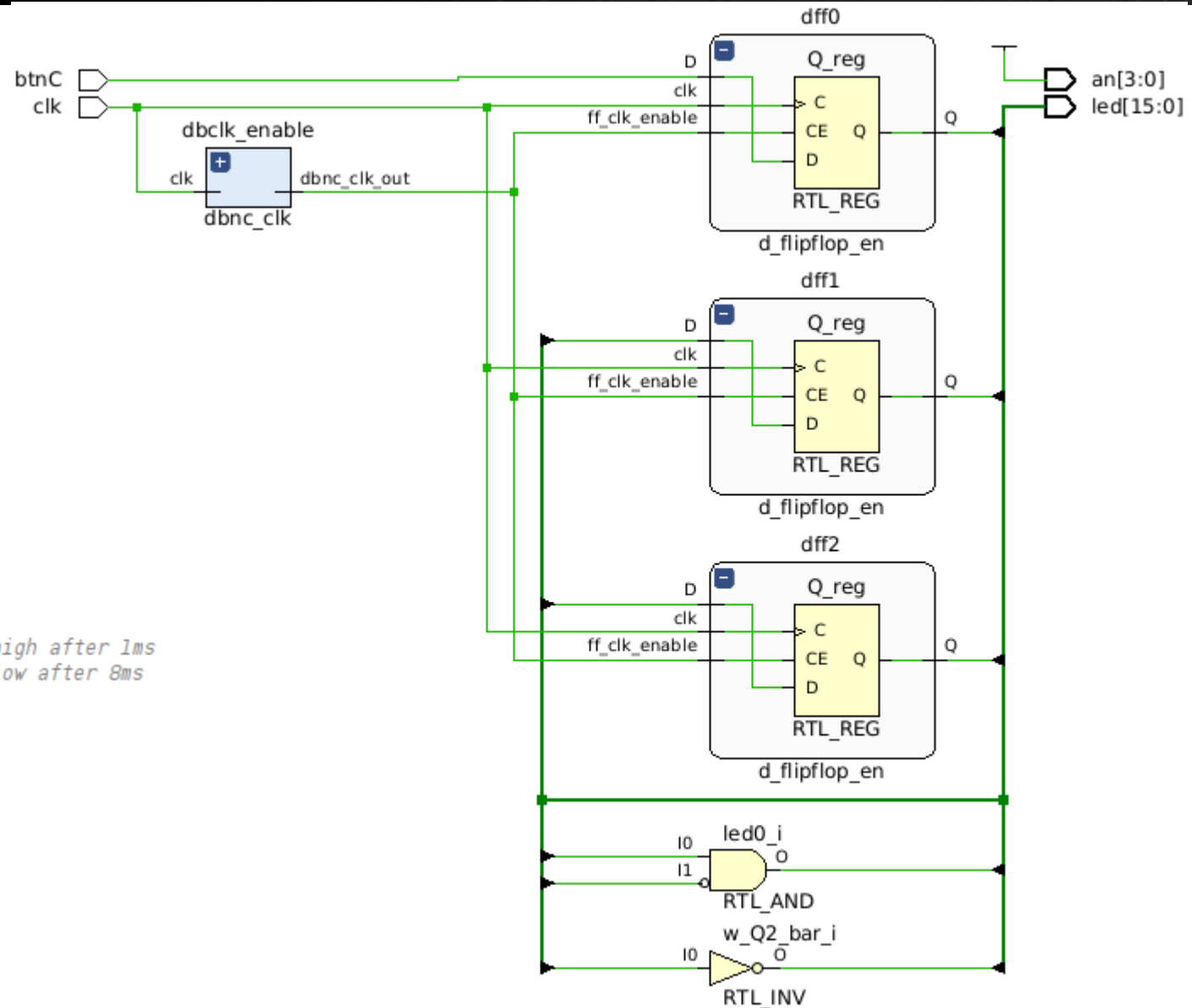


Simulation Code – tb_debounce_A.sv

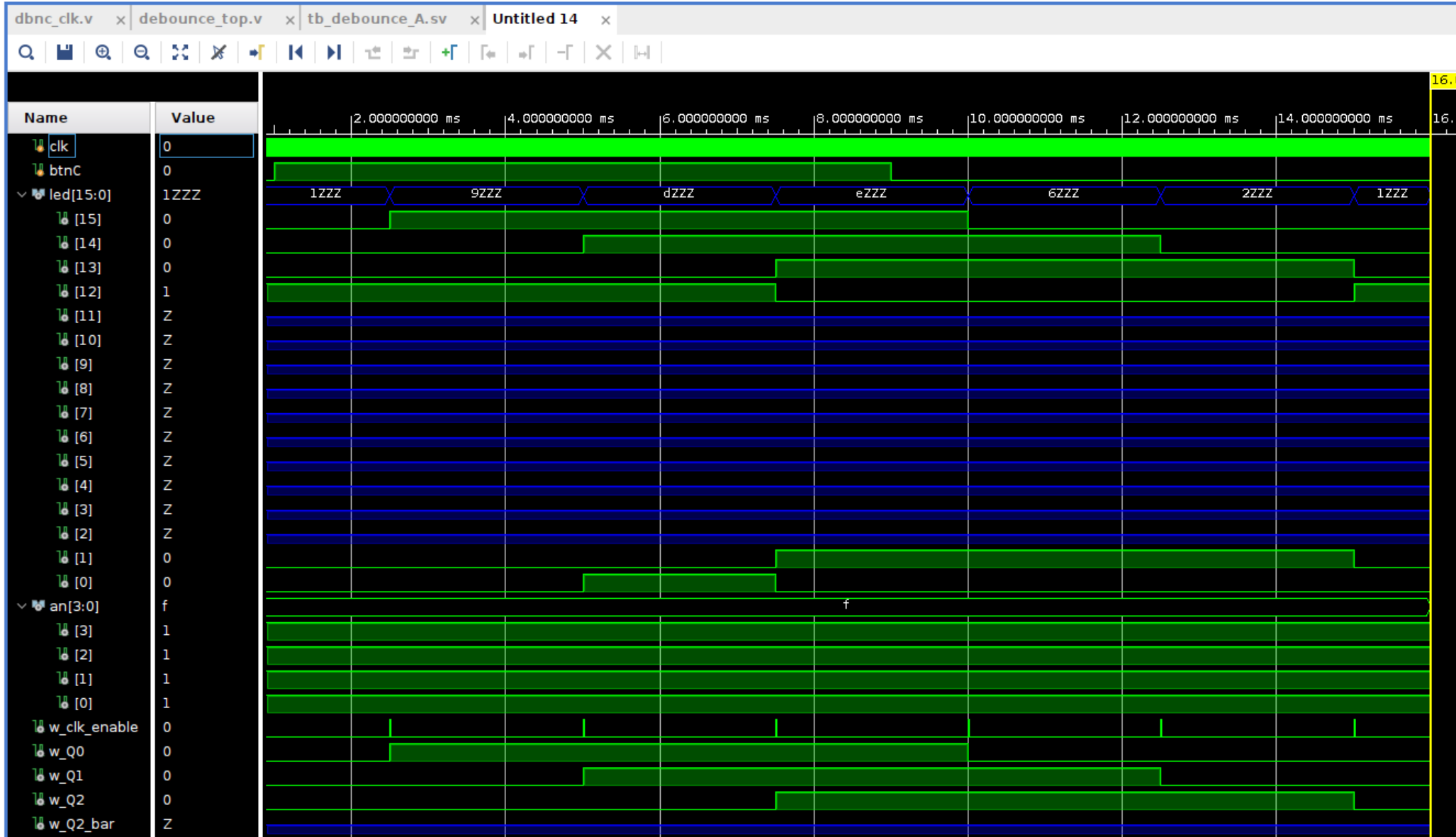
```

61 initial
62 begin
63     btnC <= 0;
64     clk <= 0;
65 end
66
67 always
68 begin
69     #5 clk <= ~clk;
70 end
71
72 initial
73 begin
74     #1000000; btnC <= 1;    //force btnC high after 1ms
75     #8000000; btnC <= 0;  //force btnC low after 8ms
76 end

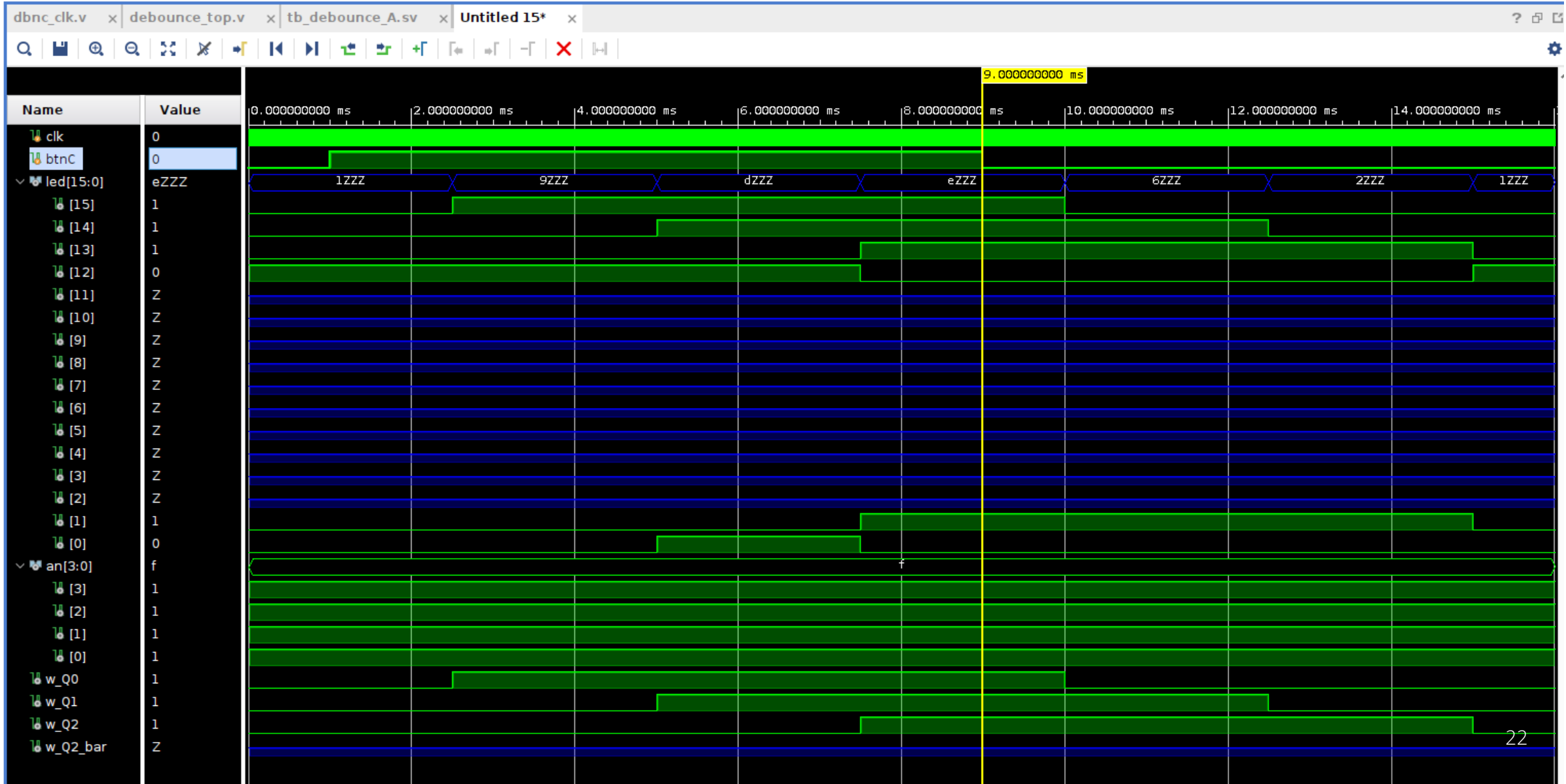
```



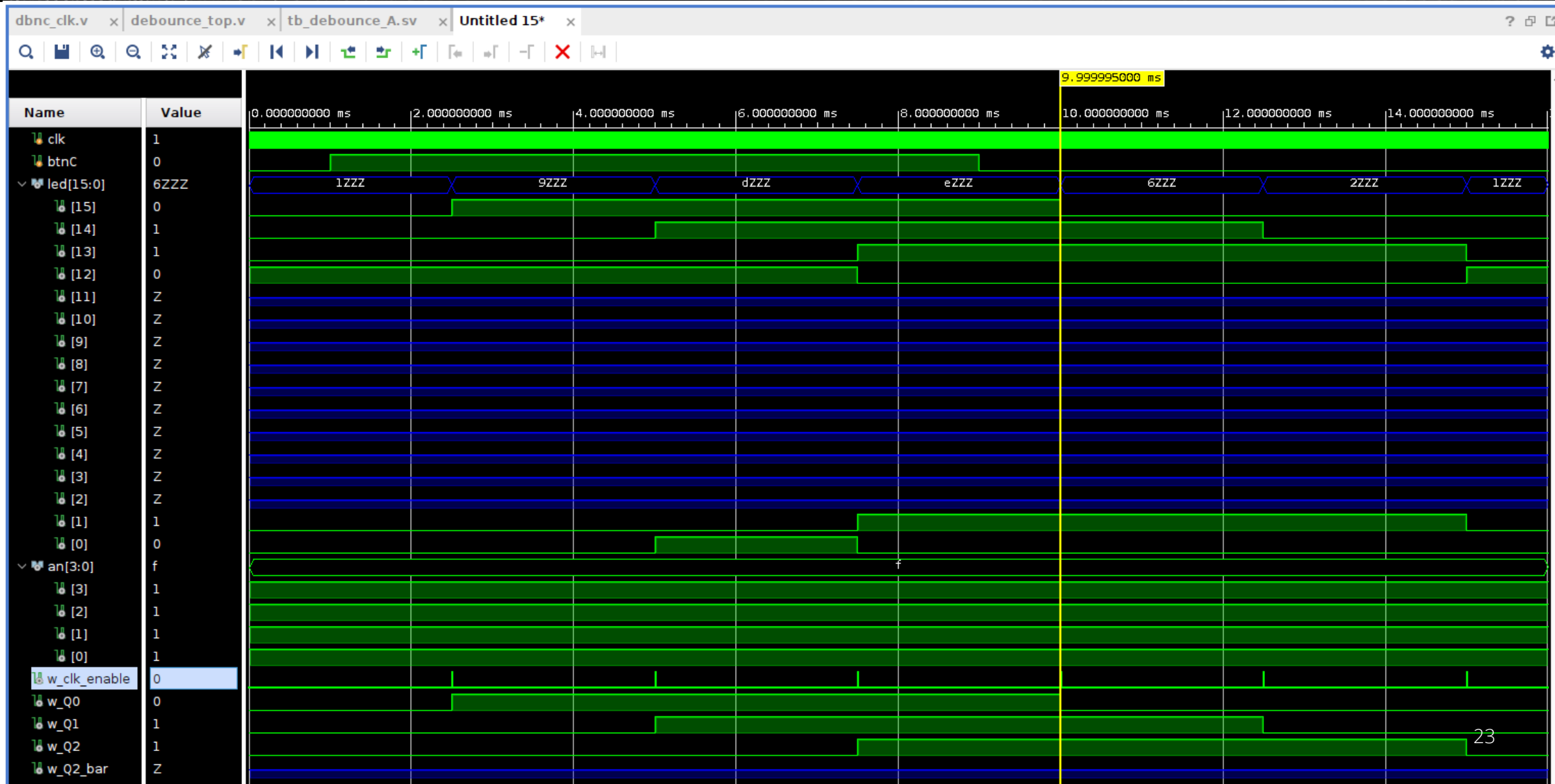
Coded Simulation Run – 16ms



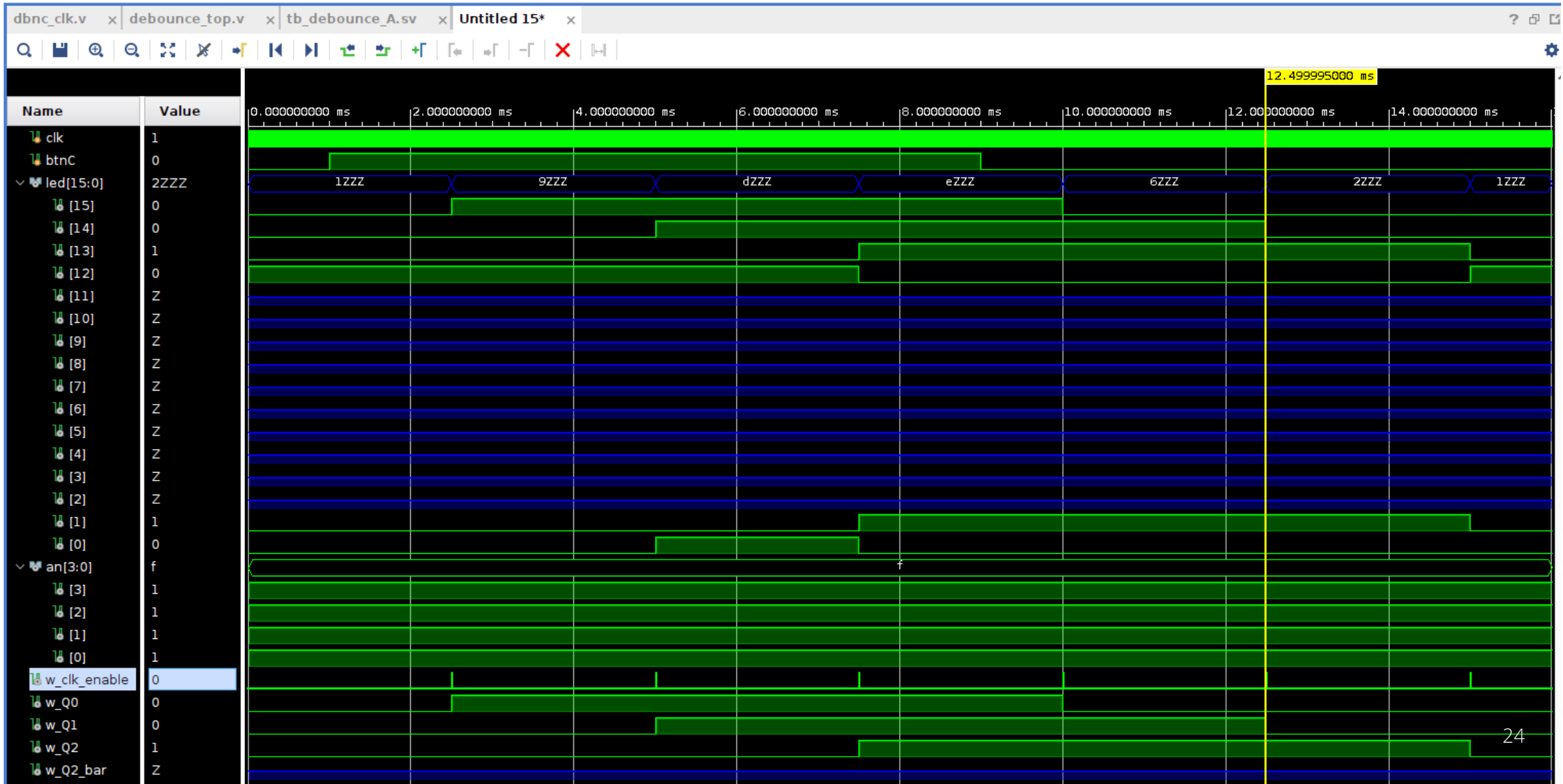
Coded Simulation Run – Release Pushbutton



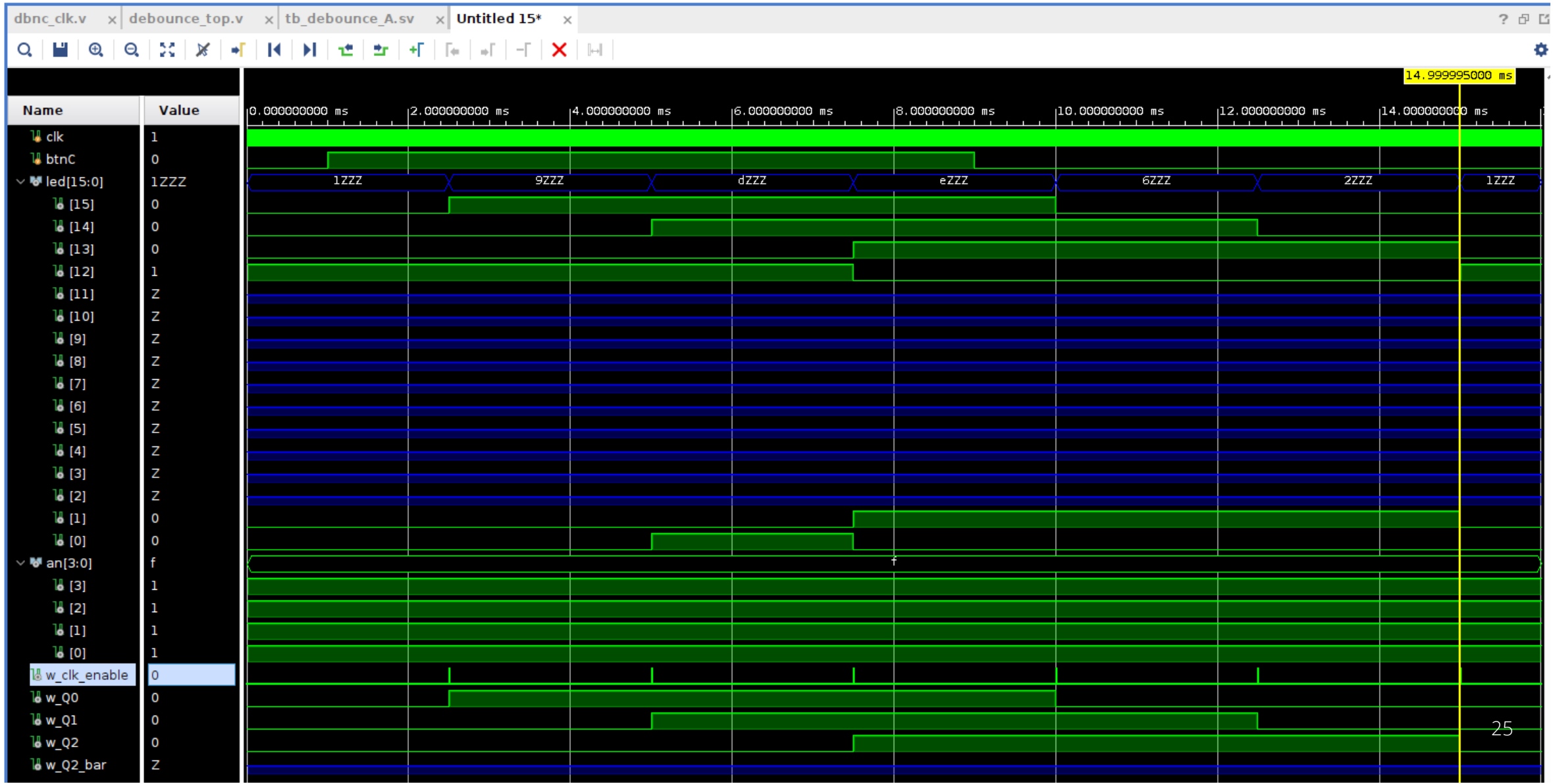
Coded Simulation Run – clk enable -1



Coded Simulation Run – clk enable -2



Coded Simulation Run – clk enable -3

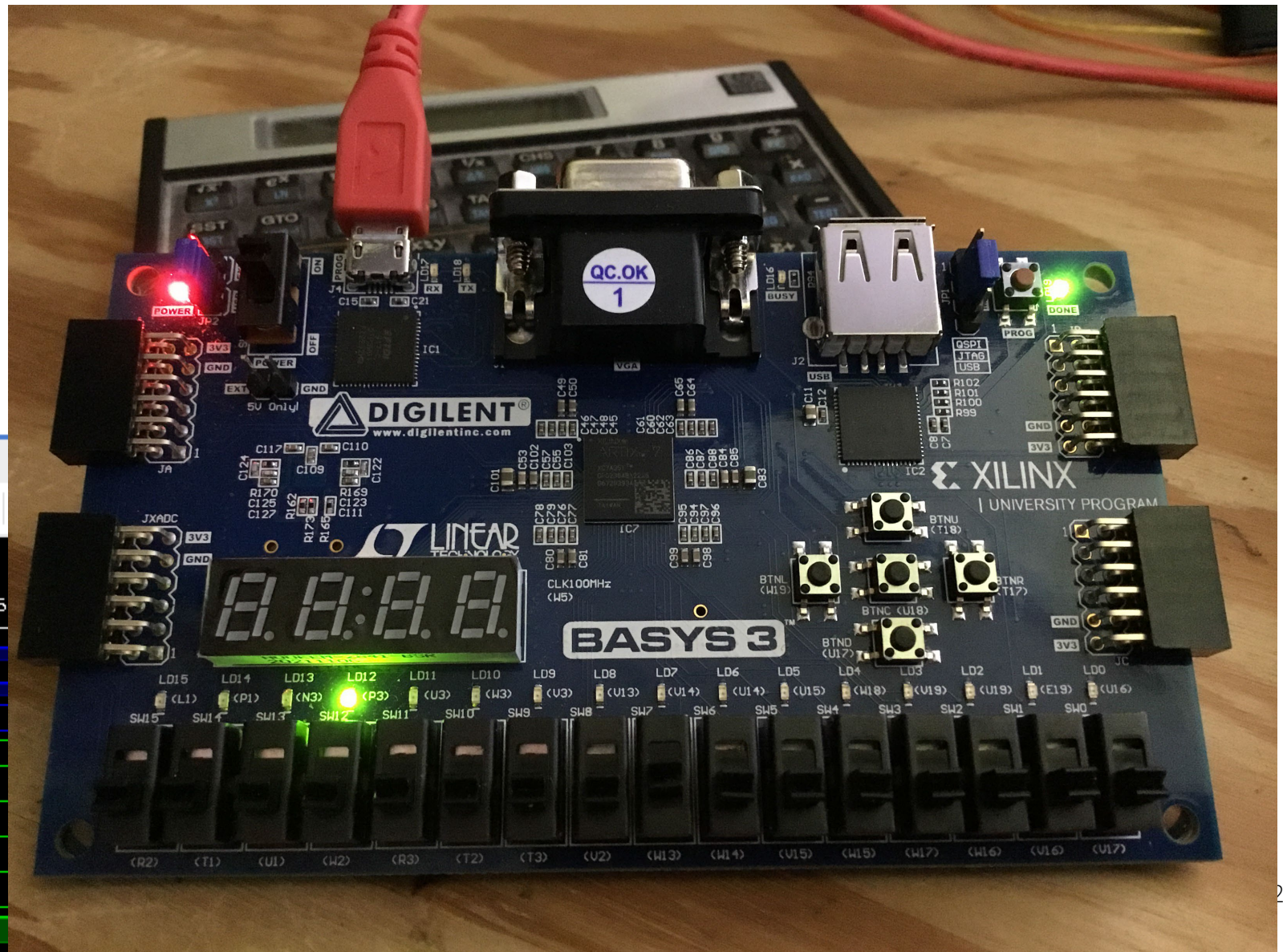


Coded Simulation End

```

57 //led[1] on as long as btnC is depressed
58 assign led[1] = w_Q2;
59 //led[0] on for 1 second
60 assign w_Q2_bar = ~w_Q2;
61 assign led[0] = w_Q1 & w_Q2_bar;
62 assign led[15] = w_Q0;
63 assign led[14] = w_Q1;
64 assign led[13] = w_Q2;
65 assign led[12] = w_Q2_bar;

```



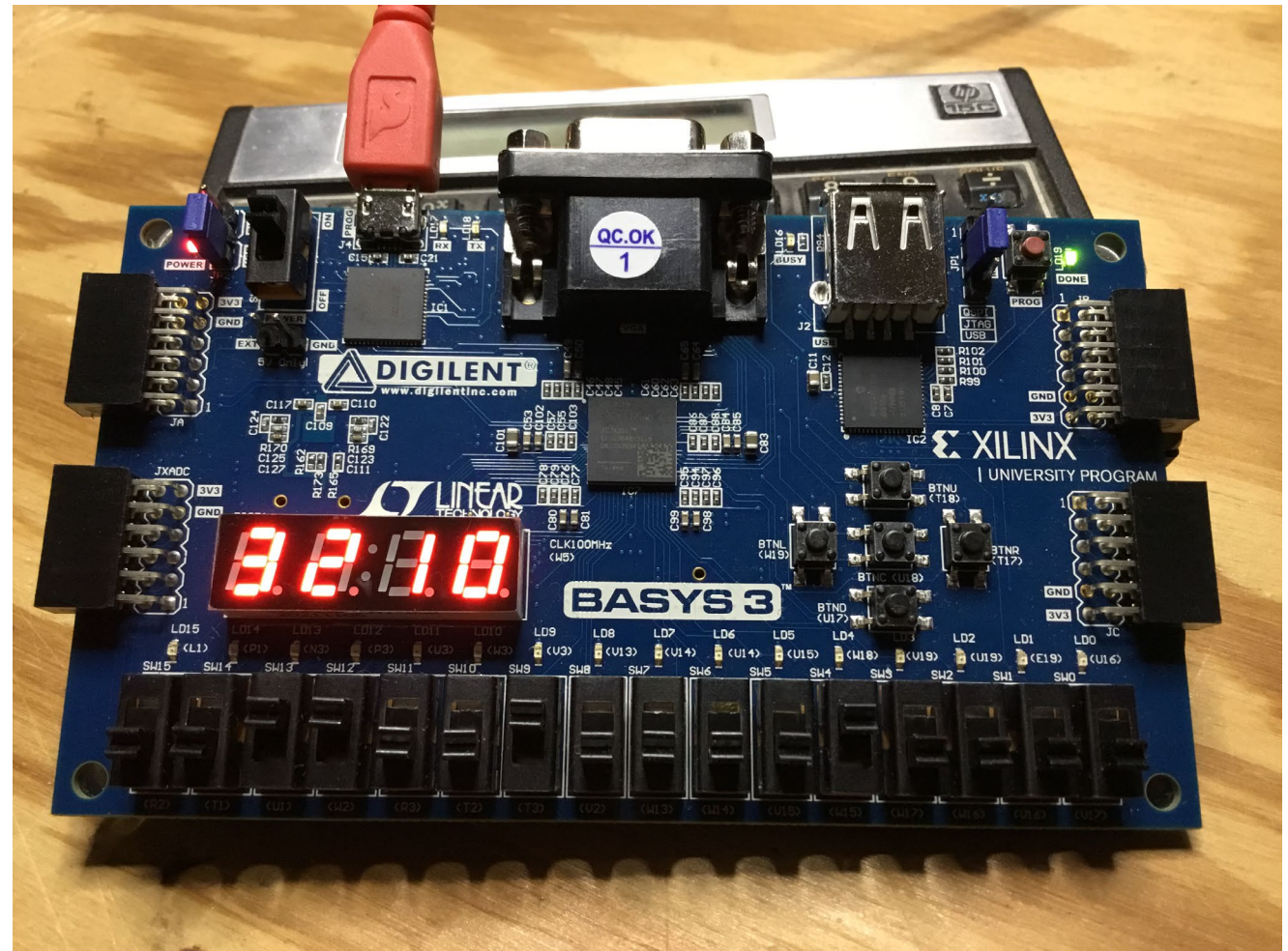
Name	Value
clk	Z
btnC	Z
led[15:0]	1ZZZ
an[3:0]	f
w_clk_enable	0
w_Q0	0
w_Q1	0
w_Q2	0
w_Q2_bar	1

MORE TO COME..

Thank you for attending!!!

Please consider the resources below:

- xilinx.com
- digilent.com
- [Basys 3 Reference Manual](#)





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