



Field-Programmable Gate Array (FPGA) Primer

Day 3: Vivado Simulation

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Fred Eady

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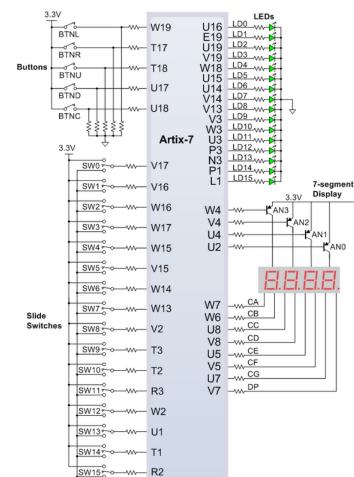
AGENDA

Simulation by Force Simulation by Code

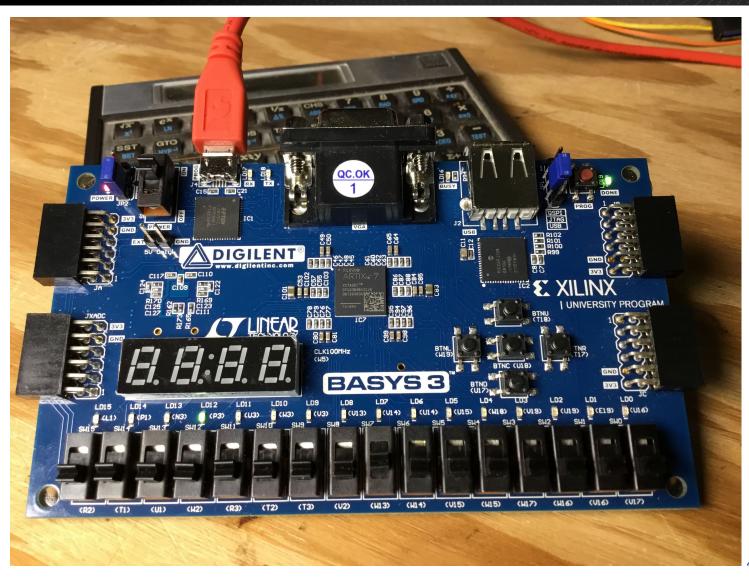
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Simulation Sources – debounce_top

7-segment Display

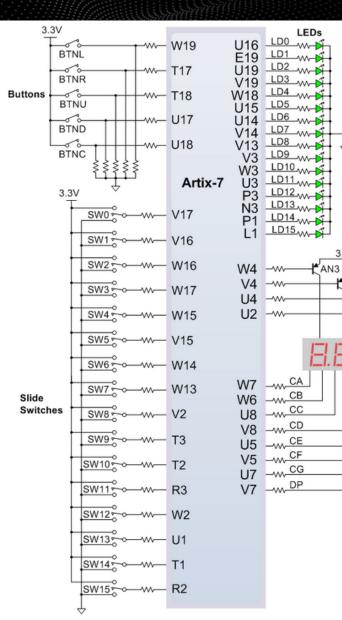
ANO

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3.3V

AN2

AN1



Flow Navigator	PROJECT MANAGER - debounce_A
> PROJECT MANAGER	Sources ? _ D 🖸 X
> IP INTEGRATOR	Q ¥ ≑ + 2 ● ○ 🌣
✓ SIMULATION	✓ □ Design Sources (1)
	> debounce_top (debounce_top.v) (4) > Constraints (1)
Run Simulation	Simulation Sources (1)
> RTL ANALYSIS	∨ 🚍 sim_l (1)
	✓ ● ∴ debounce_top (debounce_top.v) (4)
> SYNTHESIS	dbclk_enable : dbnc_clk (dbnc_clk.v)
, shahedo	dff0 : d_flipflop_en (d_flipflop_en.v)
> IMPLEMENTATION	dff1 : d_flipflop_en (d_flipflop_en.v)
	dff2 : d_flipflop_en (d_flipflop_en.v)
> PROGRAM AND DEBUG	> 📄 Utility Sources (1)
	Hierarchy Libraries Compile Order



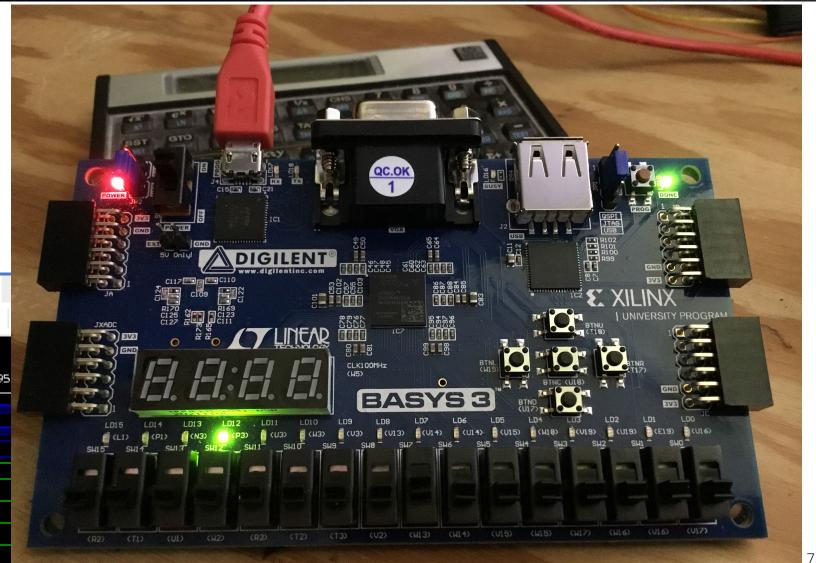
Simulation Sources – debounce_top

Flov	v Navigat	tor	≭ ≑ ? _	SIMULATION - B	ehaviora	al Simulation - Fu	Inctiona	l - sim_1 - debounce_to	p	
> PI	ROJECT M	IANAGER		Scope × So	ources	1	3 6	Objects × Protoc	coll ? _	. 🗆 🖸
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_				Name		Design Unit	B^	Name	Value	Data^
✓ SI	IMULATIO	N		debounce	_top	debounce_top	V	🕌 clk	Z	Logi
	Run Sim	ulation		📒 dbclk_e	enable	dbnc_clk	V	🕌 dbnc_clk_out	0	Logi
				📒 dff0		d_flipflop_en	V	> 😽 counter[26:0]	0000000	Arra
> R	TL ANALYS	IS		📒 dff1		d_flipflop_en	V			
				📒 dff2		d_flipflop_en	V			
> S)	YNTHESIS			📒 glbl		glbl	V			
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Q H	0. Q	Value	[1999, 998 ps 1999, 9		<mark>000,000</mark> 000,000
Name		Value			「← →「 999,99			999,998 ps 1999,9		<mark>000,000</mark> 000,000
								999,998 ps 999,9		
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Name l clk l btnC > Med[15	»:0]	Value Z Z				6 ps 999,99		999,998 ps 999,9		
Name Uck btnC Ved[15	5:0])]	Value Z Z 1ZZZ				6 ps 999,99		999,998 ps 999,9		
Name	i:0])] enable	Value Z Z 1ZZZ f				6 ps 999,99		999,998 ps 999,9 9		
Name	enable	Value Z Z 1ZZZ f 0				6 ps 999,99		999,998 ps 999,9		
Name	enable	Value Z Z 1ZZZ f 0 0				6 ps 999,99		999,998 ps 999,9 999,9 1 1 1 1 1 1 1 1 1 1 1 1 1 1		



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Forced Simulation Setup – Initial Sim Run



- 57 //led[1] on as long as btC is depressed 58 assign led[1] = w_Q2;
- 59 //led[0] on for 1 second
- 60 assign w_Q2_bar = ~w_Q2;
- 61 assign led[0] = w_Q1 & w_Q2_bar;
- 62 assign led[15] = w_QO;
- 63 ; assign led[14] = w_Q1;
- 64 assign led[13] = w_Q2;
- 65 assign led[12] = w_Q2_bar;

dbnc_clk.v x d	ebounce_top.v	/ × Untitled 6 ×
ର୍ 💾 🔍 ର୍	- 20 🗶 -	「 H H 世 世
Name	Value	999,994 ps 999,995
🕌 clk	Z	
🕌 btnC	Z	
> 👹 led[15:0]	1ZZZ	
> 👹 an[3:0]	f	
🔓 w_clk_enable	0	
™_Q0	0	
" a w_Q1	0	
" a w_Q2	0	
🛿 w 02 bar	1	



> >

Field-Programmable Gate Array (FPGA) Primer Verilog Simulation Simulation by Force

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Forced Simulation Setup – Force a Clock Signal

dbnc_clk.v × de	ebounce_top.v	/ × Untitled	16 ×					2 🗆 🖓		
ର୍ 🖬 🔍 ଭ୍ ାର୍		[€ ▶	t≛ ±r +Γ	Fe +F -F	\times III			٥		
								1,000,000 ps		
Name	Value	^{999,994} ps	999,995 ps	999,996 ps	999,997 ps	999,998 ps	999	Force Clock: /de	ebounce_top/clk	×
<pre> clk btnC w led[15:0] w an[3:0] w clk_enable w cos </pre>	Z Z 1ZZZ f 0			17	rzz f			Enter parameters below to fo constant value. Assignments code or any previously applied force will be overridden.	made from within HDL d constant or clock	A
16 w_Q0 16 w_Q1 16 w_Q2 16 w_Q2_bar	0 0 1							Signal name: <u>V</u> alue radix: <u>L</u> eading edge value:	/debounce_top/clk Hexadecimal ~ 1 ©	
								<u>T</u> railing edge value: <u>S</u> tarting after time offset: <u>C</u> ancel after time offset:	0 Cons Cons	
								Duty cycle (%): Period:	50 ÷ 10ns 100MHz clos OK Cancel	

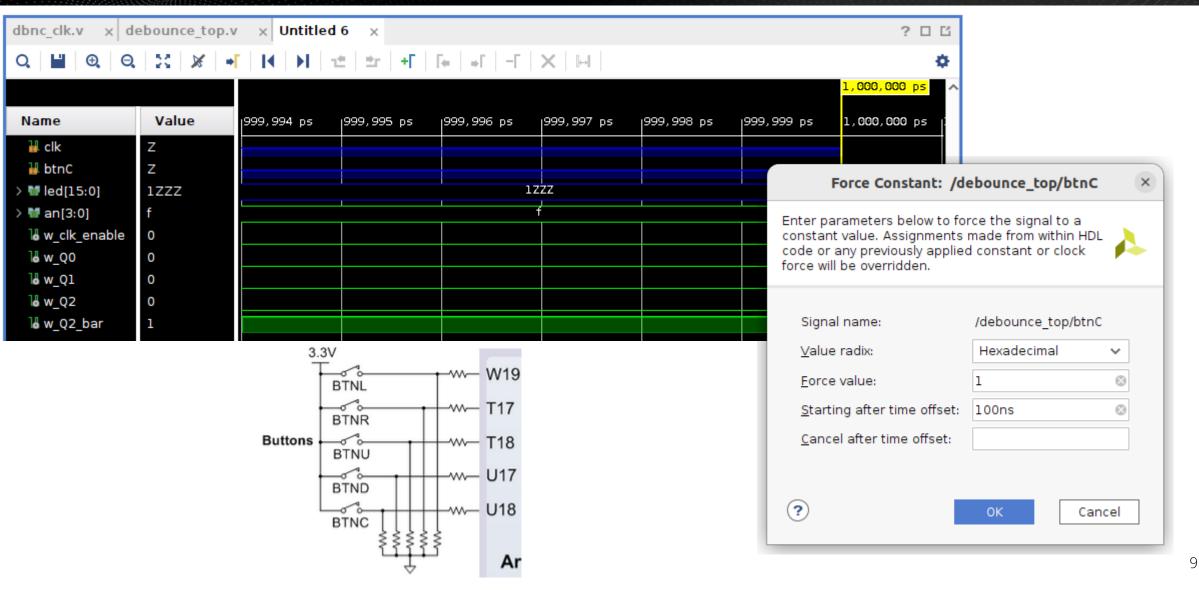
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Forced Simulation Run – 10mS

dbnc_clk.v x d	ebounce_top.v	/ × Untitled 8 ×	c			
ର 💾 ଭ୍ର	- X X +	「 I4 I>I 1± 1±	r + F F≠ →F −F	× IIII		
		0.00000000 ms				
Name	Value	0.00000000 ms	2.00000000 m≲	4.00000000 m≲	6.00000000 m≲	18.000000000 ms 10.
<mark>₩</mark> clk	Z					
₩ btnC	Z					
∨ ₩ led[15:0]	1ZZZ	1772	9zzz	χ	dzzz X	eZZZ
₩ [15]	0					
₩ [14]	0					
13]	0					
₩ [12]	1					
₩ [11]	z					
10]	z					
₩ [9]	Z					
₩ [8]	Z					
₩ [7]	Z					
₩ [6]	Z					
₩ [5]	Z					
뒚 [4]	Z					
₩ [3]	Z					
₩ [2]	Z					
₩ [1]	0					
¥ [0]	0					
∨ ₩ an[3:0]	f			f		
₩ [3]	1					
₩ [2]	1					
11 [1]	1					
¥ [0]	1					
🔓 w_clk_enable	0					
1⊌ w_Q0	0					
1 ⊌ w_Q1	0					
<mark>™</mark> w_Q2	0					
ไ₀ w_Q2_bar	1					



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Forced Simulation Run – clk enable pulse 1

dbnc_clk.v x debounce_top.v x Untitled 8 x

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				2.500990000 ms				
Name	Value	0.00000000 ms	2.000	1000000 ms	4.000000000 m≲	a. 000000000	ms	8.00000000 m≤
🕌 clk	1							
🕌 btnC	1							
∨ 🖬 led[15:0]	9ZZZ	1222		9ZZZ		dzzz		eZZZ
🕌 [15]	1							
14]	0							
🕌 [13]	0							
🕌 [12]	1							
22 [11]	z							
🕌 [10]	z							
¥ [9]	z							
🕌 [8]	z							
₩ [7]	z							
₩ [6]	z							
₩ [5]	z							
₩ [4]	Z							
₩ [3]	Z							
₩ [2]	z							
11 [1]	0							
¥ [0]	0							
~ 🖬 an[3:0]	f				f			
🕌 [3]	1							
🕌 [2]	1							
11	1							
¥ [0]	1							
🜡 w_clk_enable	0							
] ⊌ w_Q0	1							
l∎ w_Q1	0							
₩_Q2	0							
🖥 w_Q2_bar	1							



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Forced Simulation Run – clk enable pulse 2

dbnc_clk.v x debounce_top.v x Untitled 8 x

Q 📕 @ Q 🔀 🖌 📲 H 🕨 🛨 🖅 🕂 🗛 📲 - F 🗙 H

				5.00099	90000 ms		
Name	Value	0.00000000 ms	2.00000000 ms	4.000000000 m≤	6.00000000) ms	^{8.00000000} m≲
🕌 clk	1						
🕌 btnC	1						
~ 🖬 led[15:0]	dZZZ	1777	972	.z	dzzz		eZZZ
🕌 [15]	1						
14]	1						
🕌 [13]	0						
🕌 [12]	1						
🔐 [11]	Z						
🕌 [10]	Z						
🕌 [9]	Z						
🕌 [8]	z	-					
🔐 [7]	Z						
🕌 [6]	Z						
₩ [5]	z						
₩ [4]	z						
¥ [3]	Z						
₩ [2]	Z						
¥ [1]	0						
¥ [0]	1					_	
🖬 an[3:0]	f						
¥ [3]	1						
₩ [2]	1						
¥ [1]	1						
¥ [0]	1						
🜡 w_clk_enable	0						
] ⊌ w_Q0	1						
₩_Q1	1						
₩_Q2	0						
⊌ w_Q2_bar	1						



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Forced Simulation Run – clk enable pulse 3

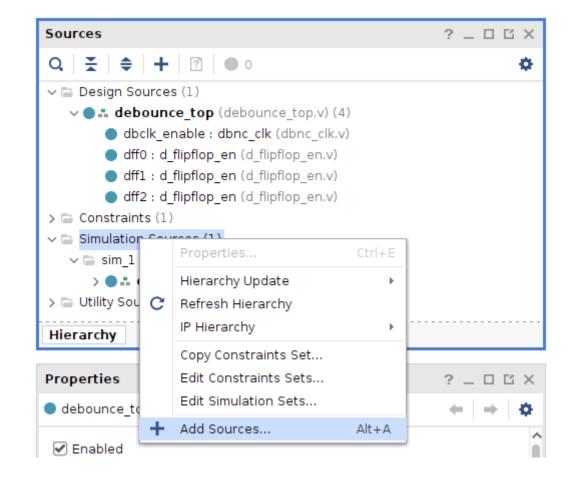
dbnc_clk.v x debounce_top.v x Untitled 8 x

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								7.500	0990000 ms
Name	Value	0.00000000 ms	2.0000	00000 ms	4.0000000	90 ms	6.00000000 ms		8.00000000 ms
🕌 clk	1								
🕌 btnC	1								
~ 🖬 led[15:0]	eZZZ	122Z		9ZZZ			dzzz		eZZZ
🕌 [15]	1								
🕌 [14]	1								
🕌 [13]	1								
🕌 [12]	0								
22 [11]	Z								
🕌 [10]	Z								
🕌 [9]	Z								
🕌 [8]	Z								
🔐 [7]	Z								
₩ [6]	Z								
🕌 [5]	Z								
₩ [4]	Z								
🕌 [3]	Z								
₩ [2]	Z								
₩ [1]	1								
¥ [0]	0								
/ 🖬 an[3:0]	f					f			
₩ [3]	1								
₩ [2]	1								
₩ [1]	1								
¥ [0]	1								
🐻 w_clk_enable	e 0								
<mark>1</mark> ∎ w_Q0	1								
<mark>™</mark> w_Q1	1								
<mark>™</mark> w_Q2	1								
🔓 w_Q2_bar	0								



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Add Sources	×
Add or Create Simulation Sources pecify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source n disk and add it to your project.	file
Specify simulation set: Create Simulation Set 🗸	
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Use Add Enter Simulation Set Name ns below Use Add Enter Simulation Set Name ns below Itb_debounce_A OK Cancel Add Files Add Directories Create File	
 Scan and add RTL include files into project Copy sources into project 	
 ✓ Add so<u>u</u>rces from subdirectories ✓ Include all design s<u>o</u>urces for simulation 	
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Id or Create Simulation Sources ecify simulation specific HDL files, or dire disk and add it to your project.	ectories containing HDL files, to add to your project. Create a new source file	^
Specify simulation set: 📄 tb_debound	e_A V Make active	
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	File type: SystemVerilog V	
	File name: tb_debounce_A File location: = <local project="" to=""></local>	
Ac	OK Cancel	
Scan and add RTL <u>i</u> nclude files into p		
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Мо	dule Definit	ion						
	<u>M</u> odule name	e: tb_debou	ince_A					\otimes
	I/O Port Def	initions						
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		input 🗸		0	0			
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?)						ОК	Cancel



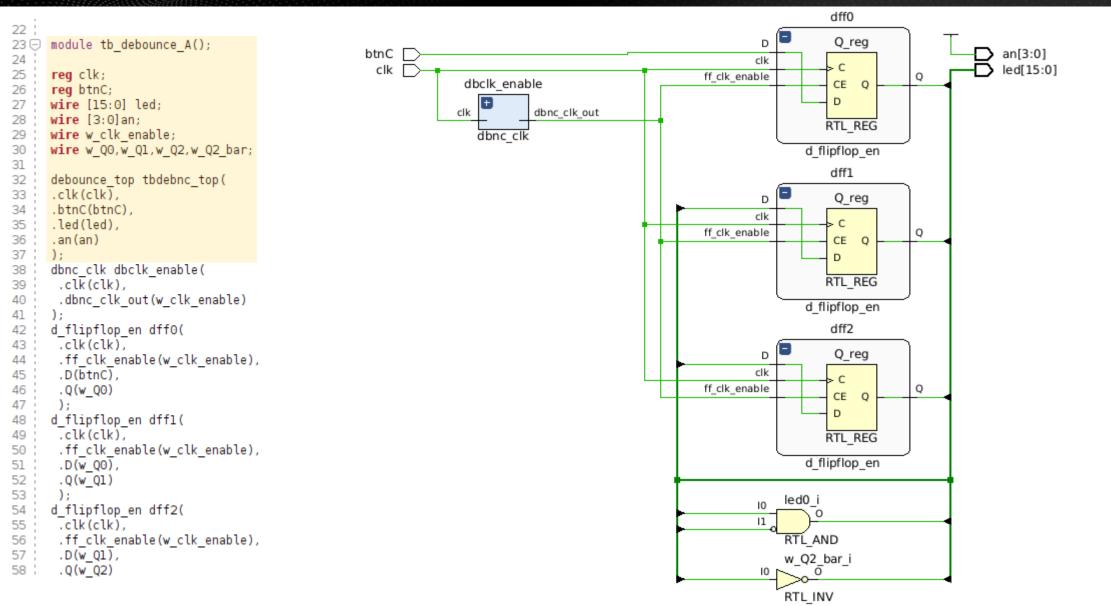
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√ □ Design Sources	(1)						
> 🔵 🚠 debounce	_top (debounce_top.v) (4)						
> 📄 Constraints (1)							
v 📄 Simulation Sour	es (3)						
∨ 🖹 tb_debound	e_A (2) (active)						
-	nce_top (debounce_top.v) (4)						
_	Source Node Properties	Ctrl+F					
∨ 📄 sim_1 (1)		Alt+0					
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> 📄 Utility Sources (Open With						
	Replace File						
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tb_debounce_A.sv	Enable File	Alt+Equal					
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🕑 Enabled	Move to Simulation Sources						
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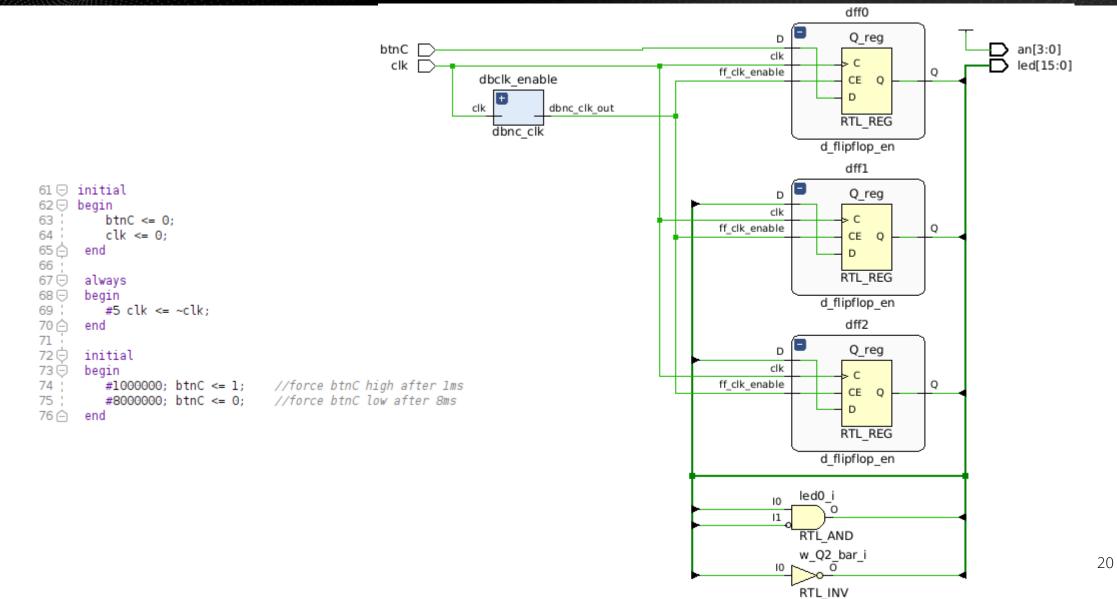
Simulation Code – tb_debounce_A.sv





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Simulation Code – tb_debounce_A.sv





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Coded Simulation Run – 16ms

dbnc_clk.v x debounce_top.v x tb_debounce_A.sv x Untitled14 x

Q | ■ | @ | Q | ☆ | ¥ | ¥ | ■ | H | ± | ± | ■ | F | F | ■ | − | × | □ |

Name	Value		2.00000000	ms	4.000000000) ms	6.00000000 ms	5	8.00000000 ms	10.00000000 ms	12.0	0000000 ms	14.00000000	00 m
🕌 clk	0													
🐌 btnC	0													
√ 😽 led[15:0]	1ZZZ	1222	<u> </u>	9ZZZ	<u>΄</u> χ		dzzz		eZZZ	6ZZZ		2222	z'χ	1Z2
16 [15]	0													
16 [14]	0													
16 [13]	0													
16 [12]	1													
16 [11]	Z													
16 [10]	Z													
[9]	Z													
16 [8]	Z													
14 [7]	Z													
16]	Z													
16 [5]	Z													
16 [4]	Z													
16 [3]	Z													
16 [2]	Z													
16 [1]	0													
16 [0]	0													
⁄ 😼 an[3:0]	f								f					
14 [3]	1													
16 [2]	1													
16 [1]	1													
] [0]	1													
😼 w_clk_enable	0													
<mark>1</mark> ⊌ w_Q0	0													
🐻 w_Q1	0													
<mark>™</mark> w_Q2	0													



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Coded Simulation Run – Release Pushbutton

dbnc_clk.v x debounce_top.v x tb_debounce_A.sv x Untitled 15* x

Q 📕 @ Q 🔀 🖌 📲 H 🕨 🛨 🖅 +F Fe eF -F 🗙 H

		9.00000000 ms											
me	Value	0.00000000 m≲	2.000000	000 ms	4.00000000 ms	6.00000000 ms		8.00000000	ms	10.00000000 ms	12.00000000 ms	14.00000000	ms
clk	0												
btnC	0												
led[15:0]	eZZZ	122	z <u> </u>	9ZZZ	<u>Х</u>	dzzz		eZZZ		6ZZZ	X	2222	1ZZZ
16 [15]	1												
14]	1												
1 [13]	1												
1 [12]	0												
🐻 [11]	Z												
1 [10]	Z												
16 [9]	Z												
16 [8]	Z												
16 [7]	Z												
🐻 [6]	Z												
16 [5]	Z												
16 [4]	Z												
1 [3]	Z												
1 [2]	Z												
1 [1]	1												
1 [0]	0												
an[3:0]	f							f					
16 [3]	1												
1 [2]	1												
16 [1]	1												
14 [0]	1												
w_Q0	1												
w_Q1	1												
w_Q2	1												
w_Q2_bar	Z												22



Field-Programmable Gate Array (FPGA) Primer Verilog Simulation Simulation by Code

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Coded Simulation Run – clk enable -1

bnc_clk.v x	debounce_top	.v x tb_debounce_A	.sv × Untitled 15*	×					?
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							<mark>9.999995000 ms</mark>		
Name	Value	0.00000000 ms	2.00000000 ms	4.000000000 ms	6.00000000 ms	8.00000000 ms	10.000000000 ms	12.00000000 ms	14.00000000 ms
😼 clk	1								
🐌 btnC	0								
🛚 😽 led[15:0]	6ZZZ	1222	9z	zz	dzzz X	eZZZ	6ZZZ	222	z 1zzz
16 [15]	0								
16 [14]	1								
16 [13]	1								
16 [12]	0								
16 [11]	z								
16 [10]	z								
16 [9]	z								
l a [8]	z								
16 [7]	z								
16]	Z								
16 [5]	z								
16 [4]	z								
l a [3]	z								
[2]	Z								
16 [1]	1								
16 [0]	0								
🔮 an[3:0]	f					f			
16 [3]	1								
1 [2]	1								
16 [1]	1								
1 6 [0]	1								
🐻 w_clk_enable	0								
₩_ Q0	0								
₩_Q1	1								
₩_Q2	1								23
₩_Q2_bar	Z								



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Coded Simulation Run – clk enable -2

dbnc_clk.v x debounce_top.v x tb_debounce_A.sv x Untitled 15* x ? 8 6 Q 📕 @ @ ∑ ∦ ୶ 🚺 № 🛨 🛨 + 🕼 → Γ 🗙 🖂 2.499995<mark>000</mark> ms Name Value 12.00<mark>0000000 ms</mark> 10.00000000 ms 12.00000000 ms 4.00000000 ms 16.00000000 ms 18.00000000 ms 10.00000000 ms 114.00000000 ms 👪 clk 0 🐌 btnC 1ZZZ 9ZZZ dZZZ eZZZ 6ZZZ 2ZZZ 1ZZZ Vec[15:0] 2ZZZ 1 [15] 0 1 [14] 0 1 [13] 1 0 6 [12] Ζ 16 [11] 1 [10] Ζ 🐻 [9] Ζ 1 [8] Ζ 1 [7] Ζ 6] 🖥 16 [5] Ζ 16 [4] Ζ Ъ [З] 1 [2] 16 [1] 1 16 [0] 0 😽 an[3:0] Ъ [З] 1 7 [2] 16 [1] 🐻 [0] & w clk enable 0 🖥 w_Q0 0 🖥 w_Q1 0 24 🖥 w Q2 1 🔓 w_Q2_bar Ζ



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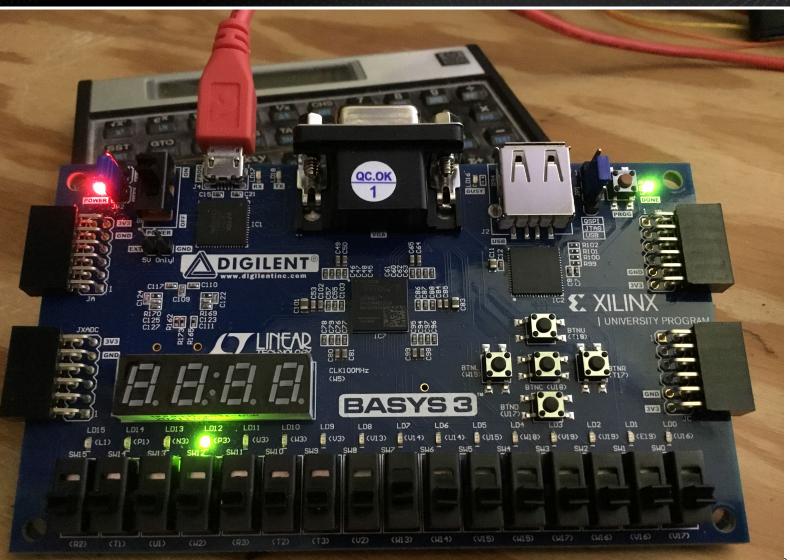
Coded Simulation Run – clk enable -3

dbnc_clk.v x d	ebounce_top.v	/ x tb_debounce_A.s	v × Untitled 15* ×						? 🗗
Q 💾 🔍 Q	20 😿 🔸	[4 >] 1± ±r	+[[+ +[-[🗙						
									14.999995000 ms
Name	Value	0.00000000 m≤	2.00000000 ms	4.00000000 ms	6.00000000 ms	18.00000000 ms	10.00000000 ms	12.000000000 ms	14.0000000 <mark>0</mark> 0 ms
🕌 clk	1								
🕌 btnC	0								
∨ 😻 led[15:0]	1ZZZ	1222	9ZZZ		dzzz X	eZZZ	6ZZZ	2222	1222
14 [15]	0								
16 [14]	0								
14 [13]	0								
16 [12]	1								
14 [11]	Z								
16 [10]	Z								
16 [9]	Z								
16 [8]	Z								
16 [7]	Z								
[6]	Z								
16 [5]	Z								
[4]	Z								
l a [3]	Z								
16 [2]	Z								
16 [1]	0								
[0]	0								
∨ 😻 an[3:0]	f								
l a [3]	1								
14 [2]	1								
14 [1]	1								
la [0]	1								
🜡 w_clk_enable	0								
<mark>™_Q</mark> 0	0								
1 ⊌ w_Q1	0								25
" a w_Q2	0								23
🐻 w_Q2_bar	Z								



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Coded Simulation End



- 57 : //led[1] on as long as btC is depressed 58 : assign led[1] = w_Q2; 59 : //led[0] on for 1 second
- 60 assign w_Q2_bar = ~w_Q2;
- 61 assign led[0] = w_Q1 & w_Q2_bar;
- 62 | assign led[15] = w QO;
- 63 | assign led[14] = w_Q1;
- 64 assign led[13] = w_Q2;
- 65 assign led[12] = w Q2 bar;

dbnc_clk.v × d	ebounce_top.	v x Untitled 6 x
ର୍ 💾 🔍 ର୍	20 🗶 -	F H H ± ±
Name	Value	999,994 ps 999,995
🕌 clk	Z	
🕌 btnC	Z	
> 🖬 led[15:0]	1ZZZ	
> 🖬 an[3:0]	f	
🛯 w_clk_enable	0	
" a w_Q0	0	
" ⊌ w_Q1	0	
" a w_Q2	0	
🔓 w_Q2_bar	1	

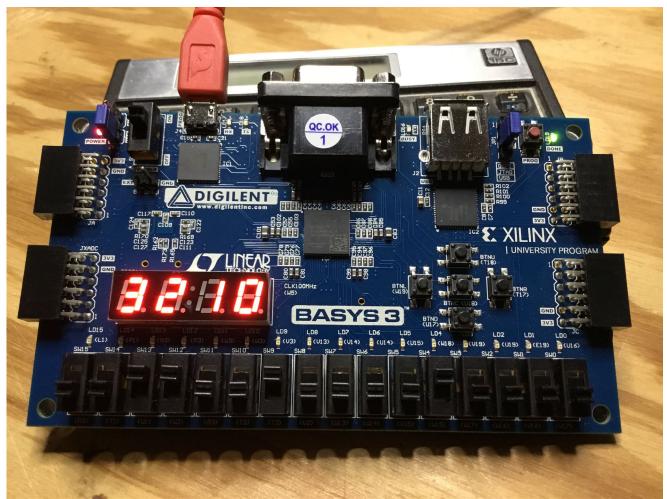


MORE TO COME..

Thank you for attending!!!

Please consider the resources below:

- xilinx.com
- digilent.com
- Basys 3 Reference Manual







Thank You





Same

