FPGA Programming

Class 4: Synthesis and Layout

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DesignNews
CEC CONTINUING EDUCATION CENTER
Presented by:
Digi-Key ELECTRONICS
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This Week's Agenda

Monday	FPGA Device Description
Tuesday	Design Flow
Wednesday	HDL
Thursday	Synthesis and Layout
Friday	Programming the Chip

Course Description

We start with an introduction to the class of devices called Field Programmable Gate Arrays (FPGAs). The layout and design of several types and critical parameters will be described and discussed. It is important to understand the way the device is constructed to develop effective algorithms.

The device we will be using this week will be the Microsemi IGLOO2. We will also discuss other devices and their structure.

We will introduce two common Hardware Description Languages (HDL), but give examples in one (Verilog).

Today's Agenda

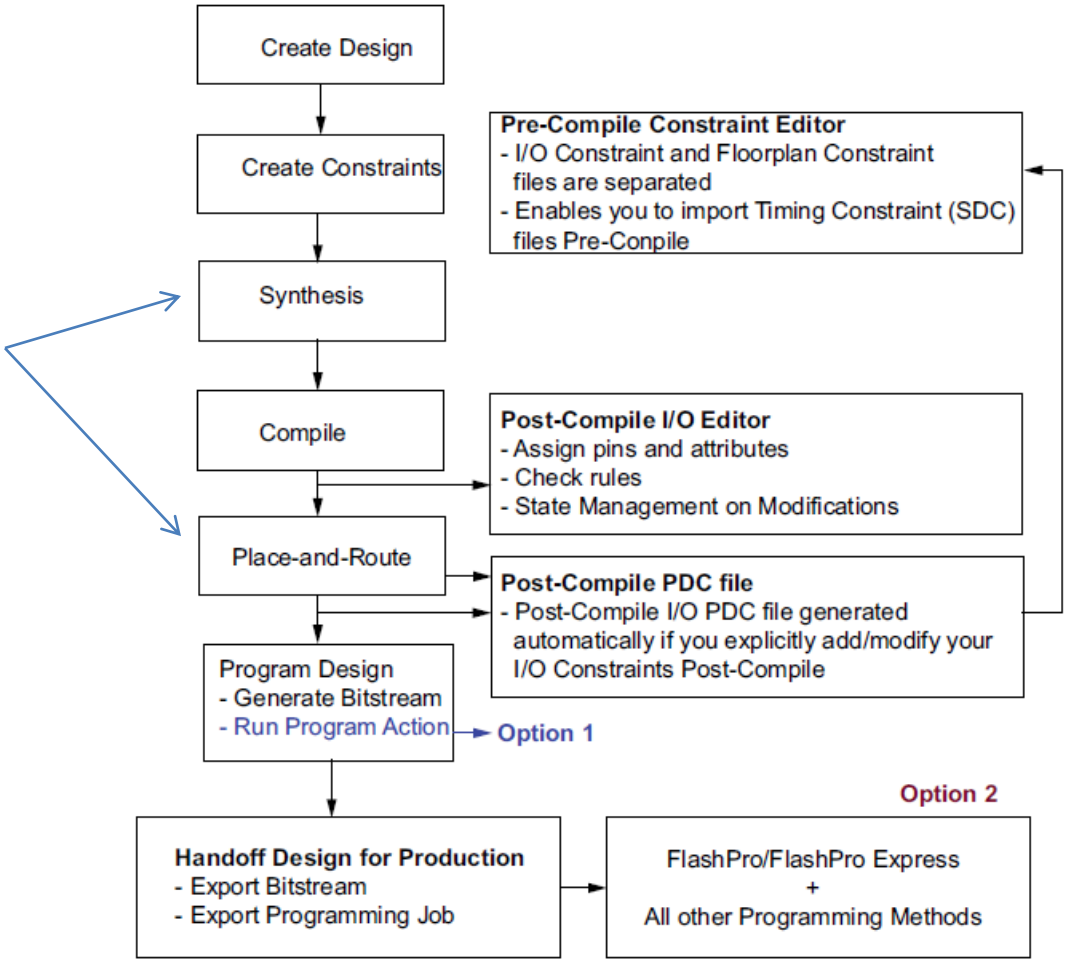
- Process Overview
- Software Tools
- Synthesis
- Layout
- Conclusion/Next Class

Process Overview

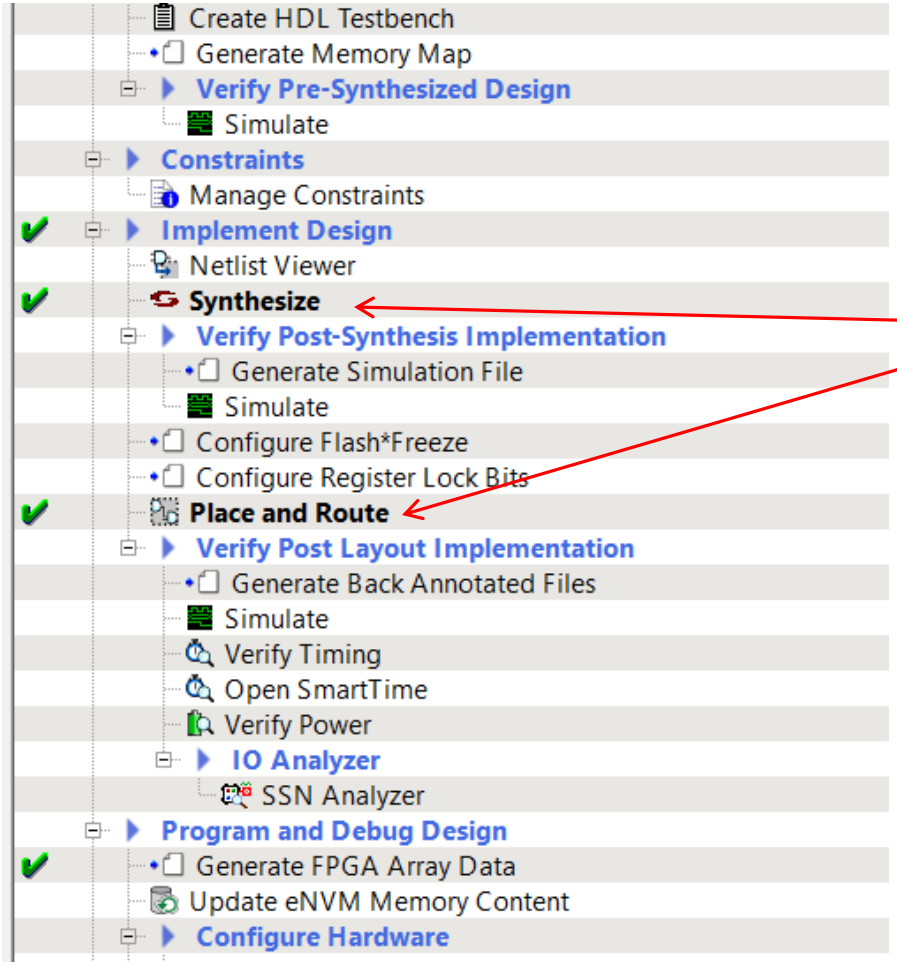
- In a typical FPGA design flow, comes after the design has been created and verified and constraints have been defined
- Examples will be given using tools from Microsemi
  - Main tool is Libero
  - We are using the latest version (11.8)

Process Overview

We are concentrating on these tasks



Process Overview



In Libero it looks like this. We will review these items.

Software Tools

- Generally vendors provide a suite of tools to develop algorithms for FPGAs
  - Xilinx: Vivado
  - Intel: Quartus
  - Microsemi: Libero
- Tool suites are expensive (several thousand $)
  - Generally include third party simulation and place and route
- Not an area where open source tool chains are generally effective

Software Tools

- Simulation tools:
  - ModelSim by Mentor Graphics is the most popular modeling and simulation tool
    - Generally included with a license tied to the particular device
- Layout tools:
  - Synplify by Synopsis is one of the more popular tools for the synthesis and layout task
  - Others can be used, in some cases not integrated

Software Tools

- The development environments also have a number of tools, that often run in different windows, to perform functions unique to the FPGA (showing Libero application names)
  - Netlist viewer: can show RTL generated
  - SmartTime: max, min and bottleneck analysis
  - Power reports (inside Libero): shows power down to the module level

Synthesis

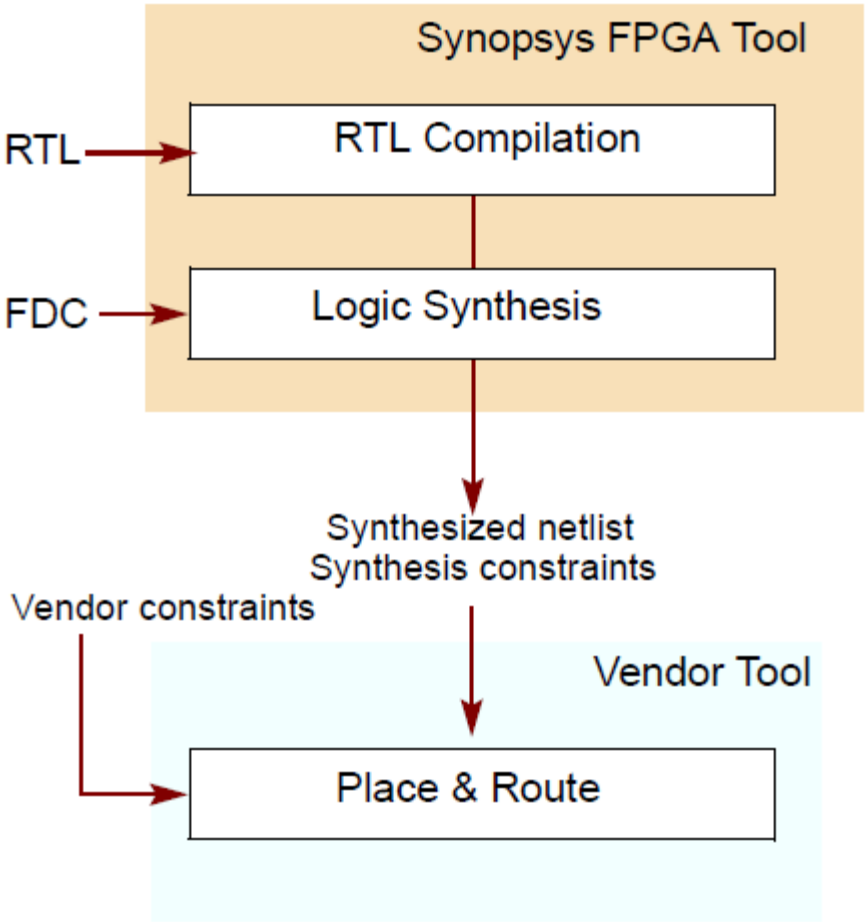
- Synthesis takes our VHDL design and produces RTL
- We will use a couple of simple applications to illustrate the tools and processes of synthesis
  - One will be a simple application to blink lights on the board
  - One uses the access to memory to observe the design process

Synthesis

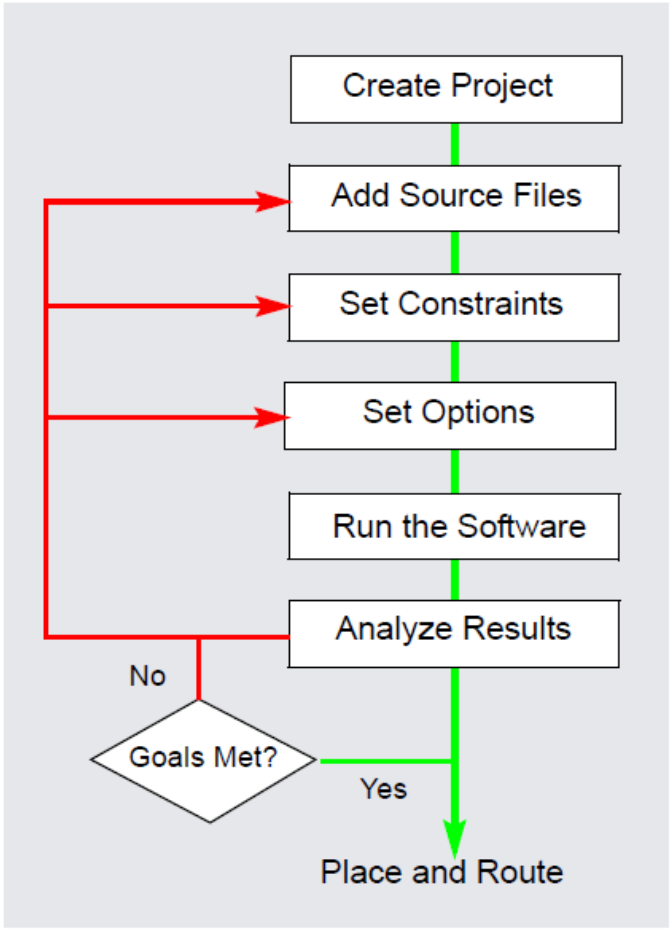
- Process
  - RTL first translated into a technology independent logic structures
  - Next these technology independent structures are mapped and optimized for the particular technology being used
  - Output is a vendor-specific netlist and constraint file that is input to the place and route tool

Synthesis

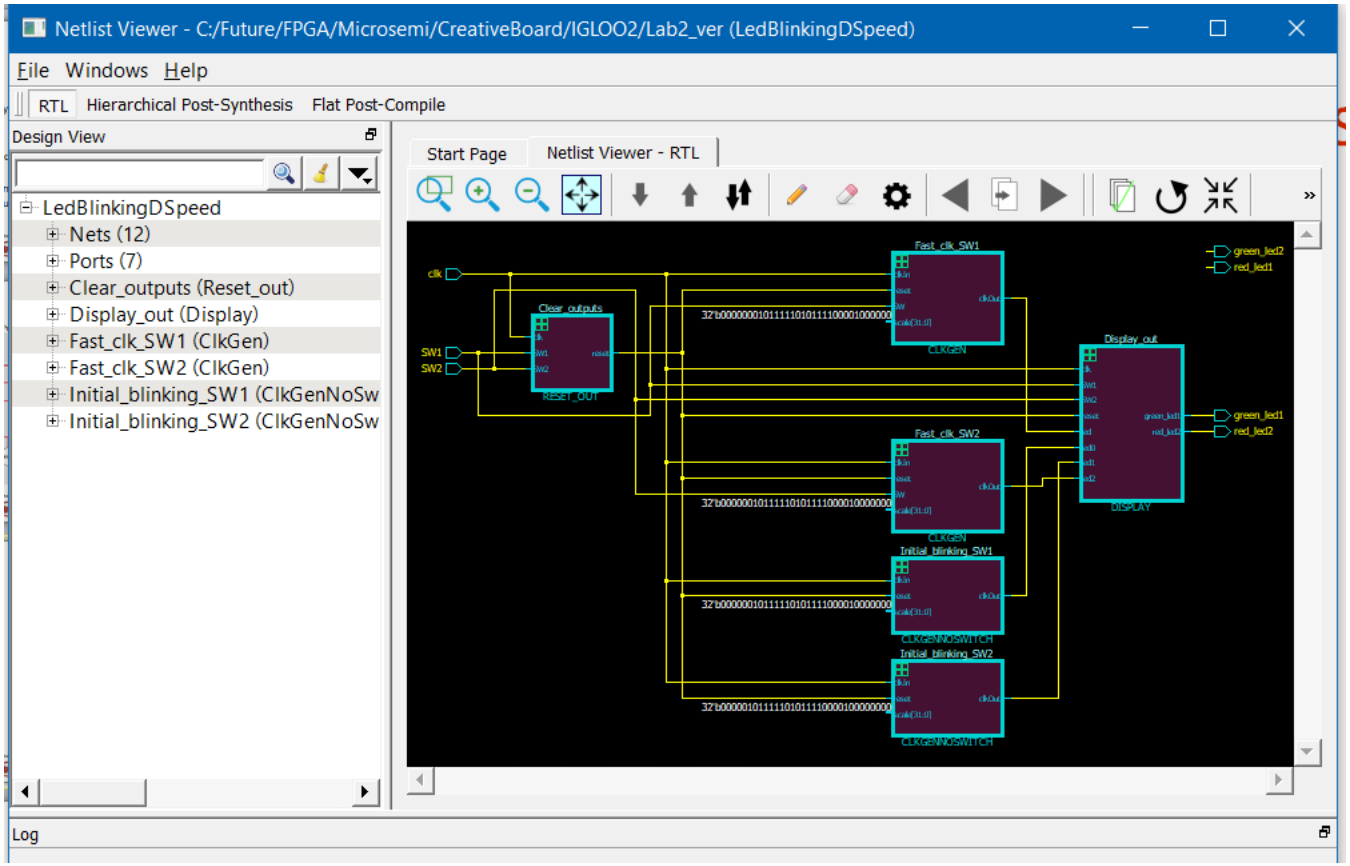
Tool Relationship



Process Flow

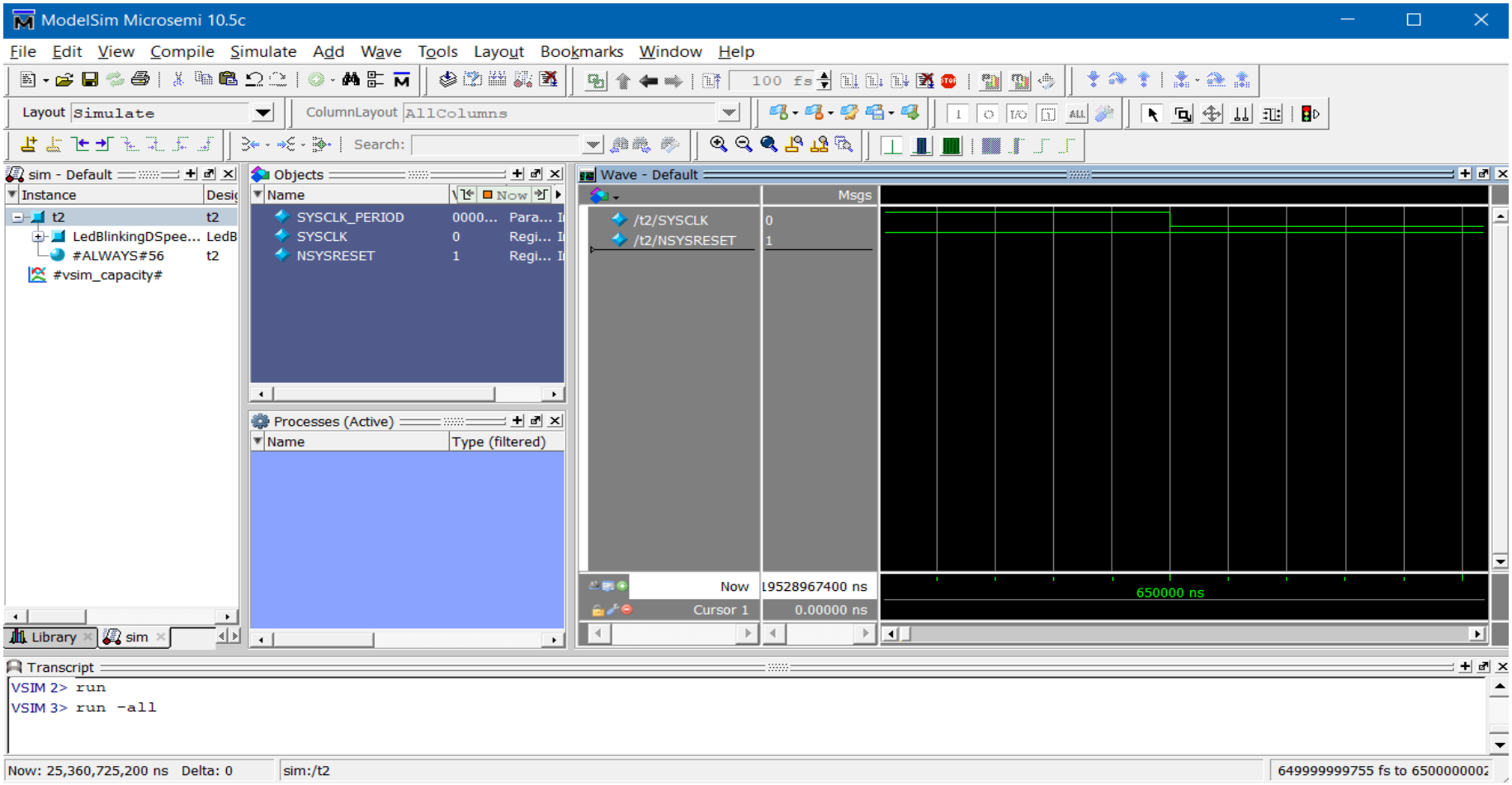


Synthesis



Netlist for a simple program that blinks lights in the board

Synthesis


ModelSim Microsemi 10.5c
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
t2
LedBlinkingDSpee...
#ALWAYS#56
#vsim_capacity#
Objects
Name
SYSCLK_PERIOD
SYSCLK
NSYSRESET
Processes (Active)
Name
Type (filtered)
Wave - Default
Msgs
/t2/SYSCLK
/t2/NSYSRESET
Now
Cursor 1
650000 ns
Transcript
VSIM 2> run
VSIM 3> run -all
Now: 25,360,725,200 ns Delta: 0
sim:/t2

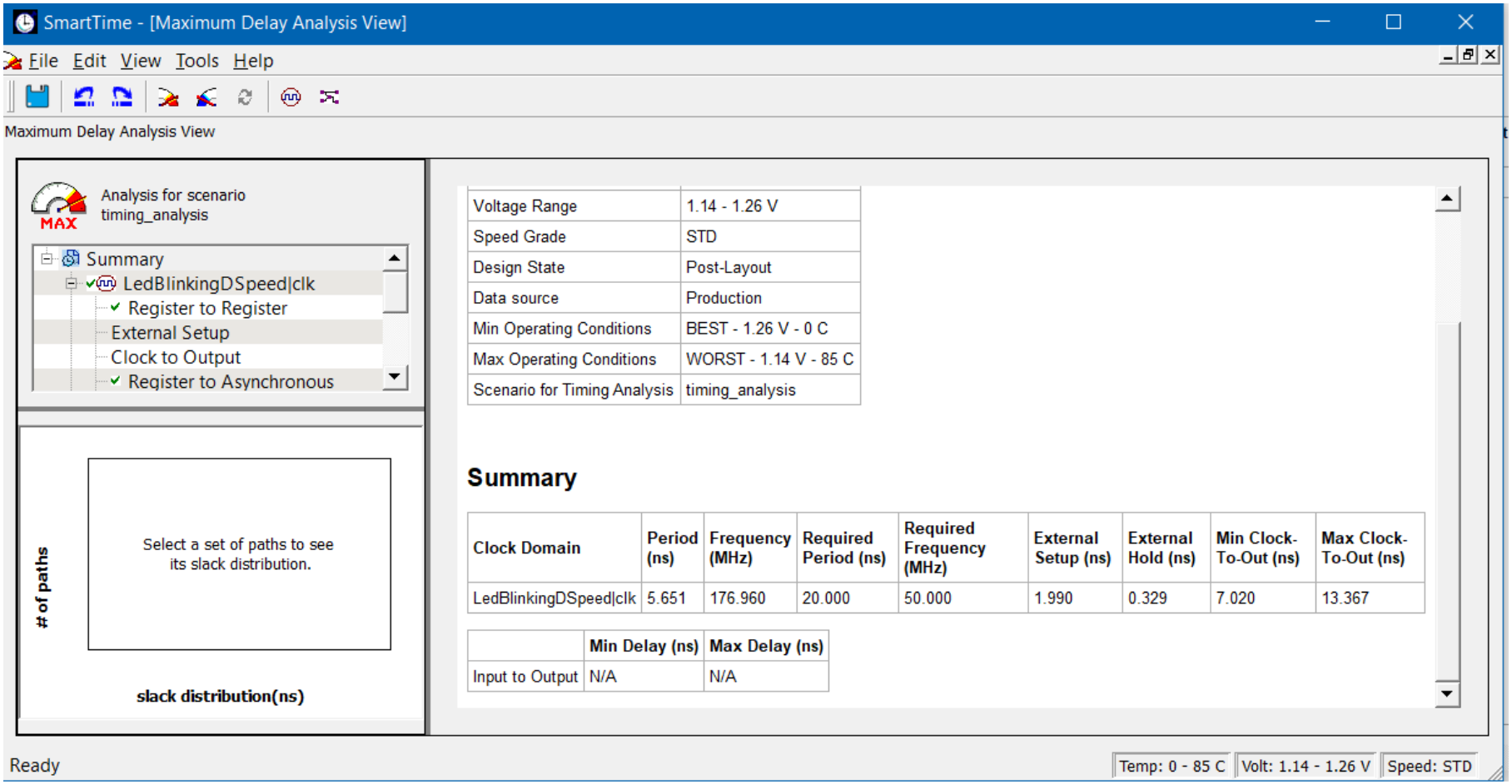
Layout

- Layout is also referred to as place and route
  - The first process of deciding where on the chip to put each circuit element
  - Next the interconnections and pathways are determined
  - This process is iterated until a design that implements the constraints is achieved

Layout

- Some of the major considerations in this step are timing and power usage
  - Tools are provided to view, in great detail, the timing and power usage of each component of the design
  - Tied back to the labels used in the HDL
- After the HDL, constraints are the most important input
  - It is the combination of our design and the constraints that make place and route work

Layout


SmartTime - [Maximum Delay Analysis View]
File Edit View Tools Help
Maximum Delay Analysis View
Analysis for scenario timing_analysis
MAX
Summary
LedBlinkingDSpeed|clk
Register to Register
External Setup
Clock to Output
Register to Asynchronous
# of paths
Select a set of paths to see its slack distribution.
slack distribution(ns)
Voltage Range 1.14 - 1.26 V
Speed Grade STD
Design State Post-Layout
Data source Production
Min Operating Conditions BEST - 1.26 V - 0 C
Max Operating Conditions WORST - 1.14 V - 85 C
Scenario for Timing Analysis timing_analysis
Summary
Clock Domain | Period (ns) | Frequency (MHz) | Required Period (ns) | Required Frequency (MHz) | External Setup (ns) | External Hold (ns) | Min Clock-To-Out (ns) | Max Clock-To-Out (ns)
LedBlinkingDSpeed|clk | 5.651 | 176.960 | 20.000 | 50.000 | 1.990 | 0.329 | 7.020 | 13.367
Min Delay (ns) | Max Delay (ns)
Input to Output | N/A | N/A
Ready
Temp: 0 - 85 C
Volt: 1.14 - 1.26 V
Speed: STD

Layout

Power Report for design LedBlinkingDSpeed with the following settings:

Vendor:	Microsemi Corporation
Program:	Microsemi Libero Software, Release Libero SoC v11.8 SP1 (Version 11.8.1.12)
	Copyright (C) 1989-
Date:	Thu Sep 14 08:35:20 2017
Version:	3.0

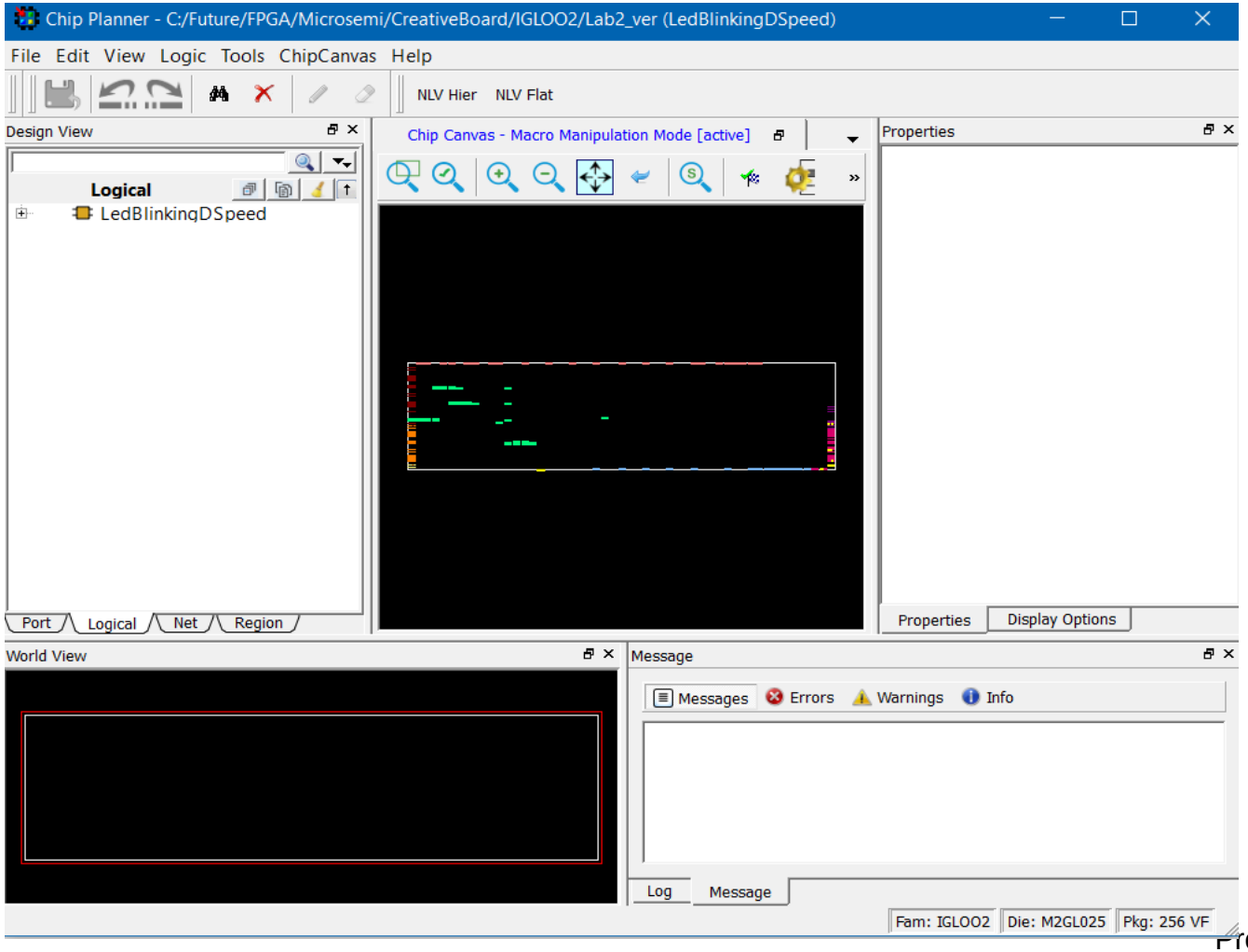
Design:	LedBlinkingDSpeed
Family:	IGLOO2
Die:	M2GL025
Package:	256 VF
Temperature Range:	COM
Voltage Range:	COM
Operating Conditions:	Typical
Operating Mode:	Active
Process:	Typical
Data Source:	Production

Power Summary

	Power (mW)	Percentage
Total Power	20.048	100.0%
Static Power	13.850	69.1%
Dynamic Power	6.198	30.9%

The system generates power reports with enough detail for the engineer to determine where power is being used, overall level and identify potential trouble spots.

Layout



As a part of the constraint process we can designate parts of the chip to be empty (so we can put a new element later) or where we want to place active elements.

Conclusion/Next Class

- Today we looked at two more steps in the FPGA design flow
  - Synthesis: design/algorithms to RTL
  - Layout: placing the synthesized design on the FPGA
- Examples from the Microsemi tool chain were used
  - Other vendors' tool chains are similar and often used the same third party tools
- Tomorrow we will get into the programming and debug processes